

Synchronous/Asynchronous Data Card Operation Manual

Channel Card for the Series KMX 9000

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STATUTORY NOTICES

APPROVALS

The SAC is approved for indirect connection to Telecommunications Systems under the General Approval number NS/G/1234/J/100003 when operated in the 9000 series multiplexer chassis. The SAC does not contain any safety isolation barriers, and any apparatus connected to it must conform with the safety requirements of the General Approval.

The Safety status of all ports is SELV.



Case Communications Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Communications Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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Synchronous/Asynchronous Data Card

1. Introduction

1.1 Synchronous/Asynchronous Data Card

The SAC is a channel interface card for installation in the KMX-9000 series range of TDM multiplexers. This manual assumes that the user is familiar with the control of the 9000 series multiplexers and installation procedures for channel cards. This manual applies to cards fitted in 9000 series multiplexers with TLM/QLM firmware V 3.00 or later. Refer to the KMX-9000 series multiplexer manual for further details.

1.1.1 General

The synchronous/asynchronous data channel card provides 4 synchronous or asynchronous data circuits. The electrical interface for all four circuits is V.28. Channel 1 is additionally switch selectable to V.11 allowing a higher speed to be used. The speed of the circuits is software selectable via the front panel.

If channel 1 is synchronous and is set to V.11 then it can be used at speeds up to 960kbps providing the rate is available on the aggregate link module (TLM or QLM) frequency PROM.

Each V.28 channel, sync or async, supports two end to end full duplex control signals which are carried in the supervisor channel of the aggregate data stream. These are RTS > DCD and DTR > DSR. The state of these signals can be forced under software control to be either High or Low as well as being transparent over the network. The CTS output reflects the RTS input at the local end. The V.11 interface supports CONTROL > INDICATE control signals.

The SAC synchronous channels are fully compatible with, and will interwork with, the HDC and DVC 9000 series channel interface cards.

2. Specifications

2.1 Synchronous Channels

Supports 4 synchronous data channels .

Electrical Interface

All channels comply with CCITT V.24/V.28. Channel 1 is switch selectable to be either V.24/V.28 or X.21/V.11.

Synchronous Data Rates

Standard data rates of 1200, 2400, 4800, 7200, 9600, 14.4k, 16k, 19.2k, 24k, 32k, 48k, 56k and 64k are supported.

Each channel can be selected independently via the front panel to be one of fourteen rates. The rates are generated within the aggregate link module, TLM/QLM, and therefore the required rate must be present in the frequency PROM. Special builds of the TLM/QLM can facilitate different sets of the available rates. Refer to the 9000 series multiplexer manual for further details.

The V.28 electrical interface is limited to 64kbps maximum subject to the length and type of cable. The V.11 interface available on Channel 1 can operate at speeds up to 960kbps.

Receive Clock

Internal - derived from the aggregate master clock.

External - at the selected data rate $\pm 0.01\%$.

Transmit Clock

Internal - derived from the aggregate master clock.

External - at the selected data rate $\pm 0.01\%$.

Receive Data Buffer

An 8bit (± 4) data buffer for removing any 'bunching' effect caused by multiplexing and allowing the use of an external receive clock. The buffer initialises to the centre when an underflow/overflow condition occurs.

Transmit Data Buffer

An 8bit (± 4) data buffer for removing any 'bunching' effect caused by multiplexing and allowing the use of an external transmit clock. The buffer initialises to the centre when an underflow/overflow condition occurs, or on the positive edge of the V.24 control signal, RTS pin 4, in half duplex applications.

2.2 Asynchronous Channels

Supports 4 asynchronous data channels .

Asynchronous Data Rates

Standard data rates of 1200, 2400, 4800, 9600 and 19.2k are supported. Only those rates included in the TLM/QLM aggregate frequency PROM can be used.

Character Format

The character length can be set under software control between 8 and 11 bits. These include 1 start, 1 or 2 stop bits and a possible parity bit.

Async Conversion Technique

CCITT rules are employed to convert transmit and receive asynchronous data to and from the synchronous format required internally by the multiplexer. No data rate compression is employed.

Async Speed Tolerance

The channels will operate within the following speed limits:- Underspeed 2.5%. Overspeed 1%. These limits may not be exceeded even if flow control is used.

2.3 Interface Control Signals

Two full duplex V.28 control signals per channel, sync and async, are transmitted within the TDM Supervisory channel. These are DTR > DSR and RTS > DCD. At the local end the RTS input controls the CTS output. The V.11 interface supports Control>Indicate control signals.

2.4 MTBF

The MTBF is 39 years calculated to HRD4.

2.5 Environmental

Operating Temperature: 0 to +40°C. Humidity: 0 to 95% non condensing.

2.6 Power Consumption

The card uses 4 watts of power. For a further breakdown refer to the chassis loading chart in section 2 of the 9000 series multiplexer manual.

2.7 Loopbacks

Individual channel loopbacks on both synchronous and asynchronous channels, which loop the receive data back to the transmit data, can be activated from the front panel. Receive data is also allowed through to the interface as normal. See figure 1-1.

Note that on the SAC Build level 1, the V.11 channel will not support loopback at data rates above 512kbps.

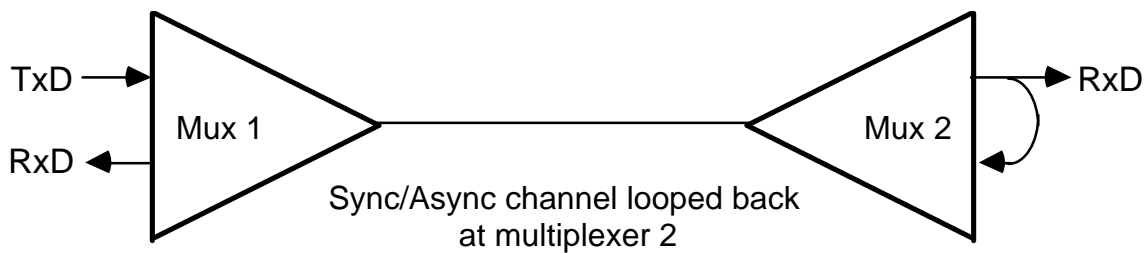


Figure 1-1 Channel loopbacks

3. Hardware Configuration

The SAC contains two configurable switches 'SW1' and 'SW2'. See figure 1-2.

SW1 is located on the rear panel and is used to select either a V.28 or V.11 electrical interface levels for channel 1. This switch is recessed from the rear panel and requires a small screwdriver or similar implement to change it. Channels 2, 3 and 4 are V.28 only.

The status of this switch is read continuously by the TLM/QLM which will determine the range of available data rates according to the interface type selected. For a V.28 interface, as with all other V.28 interfaces on the SAC the data rates are limited to 64kbps and below, whereas if V.11 is selected there is no limit imposed on the data rates other than aggregate bandwidth available to the multiplexer.

SW2 has four independent switches, S1 to S4, corresponding to channels 1 to 4. These select synchronous or asynchronous working for each channel.

OFF - SYNCHRONOUS
ON - ASYNCHRONOUS

The status of SW2 is read by the TLM/QLM which will determine the range of available data rates according to whether synchronous or asynchronous operation has been selected and the asynchronous character length available. The switch is not accessible without removing the card.

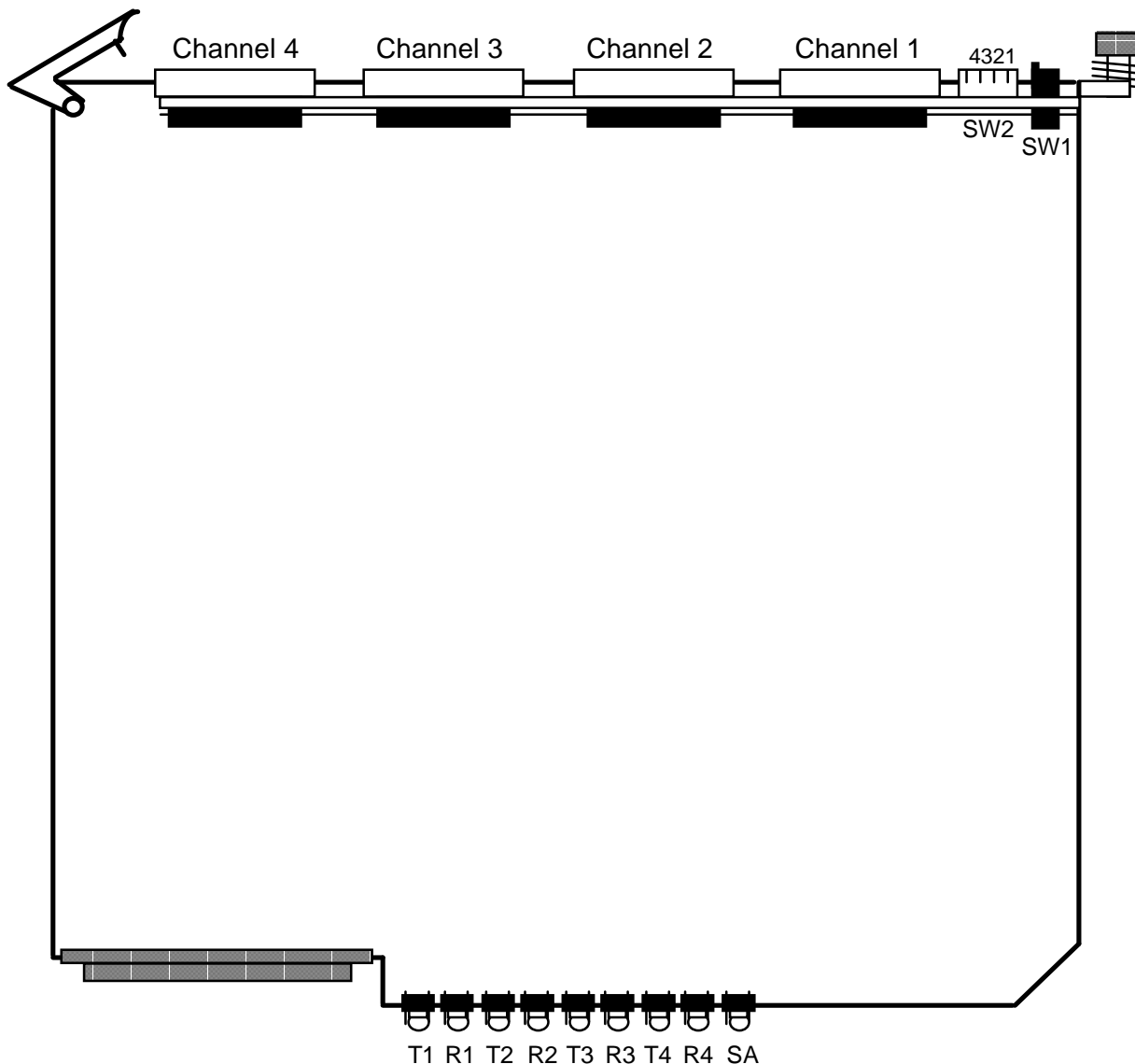


Figure 1-2 SAC Board Layout

4. Software Configuration

4.1 Data Rate

After configuring the aggregate port from the main 9000 menu, 'ADD NEW CHANNEL' should be selected and a SYNC or ASYNC (SAC) channel selected. The data rate can then be altered by using the UP and DOWN keys. The entry below the lowest rate (or above the highest) being 0K DELETE CHANNEL which allows the user to remove the channel from the configuration. If 0K is selected by pressing the ENTER key, the parameters for the next channel in the configuration will then be displayed.

4.2 Remote Channel Address.

Having determined the data rate, the next display facilitates selection of the remote channel address:-

```
CH nn REMOTE
ADDRESS mm
```

The current remote channel address is displayed on the second line and the user scrolls through the possible addresses using the UP and DOWN keys to select the required address.

4.3 V.24 Control States.

The transmit V.24 control states may be set as follows:-

```
CHnn TX CONTROLS
C1P C2L
```

C1 controls the remote DCD, C2 controls the remote DSR, C3 and C4 are not used by this card and should be ignored.

The second line gives the state of each of the V.24 controls (P = Pass, H = forced High, L = forced Low). The user can alter each state in turn starting with C1 by pressing the ENTER key and then using the UP and DOWN keys to change the state: the current control state being denoted by a '?' to the right of it. Repeated selection of the ENTER key will leave the states as they were.

The V.24 control and channel clocking attributes for the new channel are transferred from the old channel at the remote multiplexer if it was previously configured.

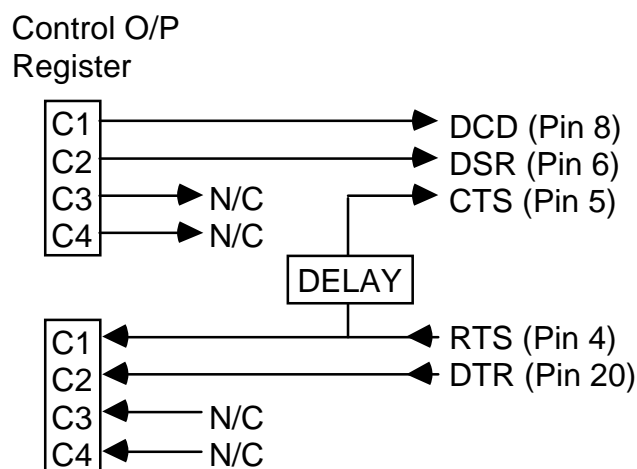


Figure 1-3 V.24 Control Paths

CTS is derived from the incoming RTS signal. The CTS low to high transition will follow the RTS input but will be delayed by a variable amount selected by changing a resistor value for each channel on the card as follows: R21 = Chan1, R24 = Chan2, R28 = Chan3 and R31 = Chan4.

| RTS/CTS Delay in ms. | E96 Resistor value in kohms. |
|----------------------|------------------------------|
| 1 | 5.10 |
| 10 | 34.0 |
| 25 | 90.9 |
| 50 | 200 |
| 100 | 536 |
| 253 | Not fitted |

4.4 V.11 Control States - Channel 1 only

Control (C) and Indicate (I) control signals are supported. The I output can be set to Pass, High or Low with the C1 control. C2, C3 and C4 are not used.

4.5 Internal/External Channel Clocks.

The selection of channel clocks is applicable to synchronous channels only. The following display is presented:-

```
CH nn CLOCKS
TX INT RX INT
```

The UP and DOWN keys are used to select the appropriate configuration as displayed on the second line:-

```
TX INT RX INT
or TX EXT RX INT
or TX EXT RX EXT
```

Pressing ENTER will confirm the selection.

The Local V.24 handshake outputs are configured by accessing the channel at the remote end of the connection. When adding a new channel the V.24 attributes and clocking parameters for the remote multiplexer are set to the default conditions, i.e. both clocks internal and both V.24 controls forced high.

When the Tx and Rx clocks are both set to EXT, it is only necessary to connect an incoming clock to pin 24 of the 25 way 'D' type since the Tx and Rx buffers are clocked from the same source under these conditions.

4.6 Bits/Character Length (Async only)

The bits/character for an async channel can be set. Having set up the channel rate, remote channel address and V.24 attributes the following display is presented:

```
CH xx  
BITS/CHAR = n
```

where 'n' is the number of bits/character i.e. 8, 9, 10 or 11 which includes start bit, stop bit(s) and a parity bit.

When adding a channel, the default setting at the remote end of the connection is 10 bits/character and can be changed by remotely accessing the multiplexer.

5. LED Status Indicators

- T1** when illuminated indicates space polarity for transmit data on channel 1.
- R1** when illuminated indicates space polarity for receive data on channel 1.
- T2** when illuminated indicates space polarity for transmit data on channel 2.
- R2** when illuminated indicates space polarity for receive data on channel 2.
- T3** when illuminated indicates space polarity for transmit data on channel 3.
- R3** when illuminated indicates space polarity for receive data on channel 3.
- T4** when illuminated indicates space polarity for transmit data on channel 4.
- R4** when illuminated indicates space polarity for receive data on channel 4.
- SA** indicates card type, SA for SAC should be permanently illuminated if the card is inserted and the power is applied to the chassis.

6. Channel Interface I/O Connections

25 way 'D' type socket. Configured for CCITT V.24/V.28 DCE

| Pin No. | Signal Name | Direction |
|----------------|---------------------|------------------|
| 1 | Protective ground | - |
| 2 | Transmit data | To Mux |
| 3 | Receive data | From Mux |
| 4 | Request to send | To Mux |
| 5 | Clear to send | From Mux |
| 6 | Data set ready | From Mux |
| 7 | Common return | - |
| 8 | Carrier detect | From Mux |
| 9 | + 12V | From Mux |
| 10 | - 12V | From Mux |
| 15 | Int Transmit clock | From Mux |
| 17 | Receive clock | From Mux |
| 20 | Data terminal ready | To Mux |
| 24 | Ext Transmit clock | To Mux |

25 way 'D' type socket. Configured for CCITT V.11 DCE (channel 1 only)

| Pin No. | Signal Name | Direction |
|----------------|----------------------|------------------|
| 1 | Protective ground | - |
| 23 | Transmit data A | To Mux |
| 10 | Transmit data B | To Mux |
| 16 | Receive data A | From Mux |
| 14 | Receive data B | From Mux |
| 7 | Common return | - |
| 9 | +12V | From Mux |
| 19 | Indicate A | From Mux |
| 18 | Indicate B | From Mux |
| 22 | Int Element timing A | From Mux |
| 21 | Int Element timing B | From Mux |
| 13 | Control A | To Mux |
| 25 | Control B | To Mux |
| 12 | Ext Element timing A | To Mux |
| 11 | Ext Element timing B | To Mux |

7. Interface Connecting Cables

The following Interface cable assemblies are available from your supplier:

| | |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Code 1525-XXX | Cable assembly D25P-D25P. V.24 to V.24 (DCE) modem. Clocks supplied to/from the modem. |
| Code 1526-XXX | Cable assembly D25-D15P. V.11 (port 1) to X.21 NTU (DCE). Clock supplied from the NTU. |
| Code 1530-XXX | Interface converter/cable D25P-D15P. V.24 to V.11 (DCE) Not required for channel 1. Clock supplied by the DCE. |
| Code 1531-XXX | Cable assembly D25P-D25S. V.24 to V.24 (DTE). Clock supplied to the DTE. |
| Code 1532-XXX | Interface converter/cable D25P-D15S. V.24 to V.11 (DTE) Not required for channel 1. Clock supplied to the DTE. |
| Code 1533-XXX | Cable assembly D25P-D15S. V.11 (port 1) to V.11 (DTE). Clock supplied to the DTE. |
| Code 1536-XXX | Cable assembly D25P-D37P. V.11 (port 1) to V.36 NTU (DCE). Clock supplied from the NTU. |
| Code 1537-XXX | Cable assembly D25P-D37S. V.11 (port 1) to V.36 (DTE). Clock supplied to the DTE. |
| Code 1538-XXX | Interface converter/cable D25P-D37P. V.24 to V.36 (DCE) Not to be used with channel 1. Clock supplied by DCE. |

Code 1539-XXX Interface converter/cable D25P-D37S.
V.24 to V.36 (DTE) Not to be used with channel 1.
Clock supplied to the DTE.

XXX denotes the cable length in metres: to be specified on order. Standard cable length of 2 metres will be supplied (i.e. 002), if not specified.

