

8 Channel 2/4 Wire ADPCM Card Operating Information

© Case Technology Ltd 1997

STATUTORY NOTICES



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

Case Technology Limited has made all reasonable efforts to ensure the accuracy of the content of this document but the information contained herein does not constitute a warranty of performance of the equipment and/or software described and no specifications given form part of any contract. This document does not constitute a licence to use or copy any software described herein and any such software must only be used in accordance with the terms of the licence supplied herewith.

Case Technology Limited reserves the right to make alterations to the equipment and software described without notice and assumes no liability for any loss or damage caused as a result of use of this document whether because of out of date or inaccurate information or otherwise.

Product and manufacturers' names referred to in this document are used for identification purposes only and Case Technology Limited acknowledges the intellectual property rights of their respective owners in the same.

This document is the copyright of Case Technology Limited and may not be reproduced, copied or stored in any computerised retrieval system by any means without the express written permission of Case Technology Limited.

Published by Case Technology Technical Publications Department

STATUTORY NOTICES

APPROVAL

- 1) This card is only approved for use in the Case 3000 series multiplexer chassis. The approval number is NS/3660/12/H/452538.
- 2) WARNING. Interconnection directly, or by way of other apparatus, of ports marked:-
"WARNING. CONNECT ONLY APPARATUS COMPLYING WITH BS6301 TO THIS PORT"
or
"WARNING . CONNECT ONLY APPARATUS COMPLYING WITH BS6301 TO THESE PORTS"
with ports not so marked may produce hazardous conditions on the network. Advice should be obtained from a competent engineer before such a connection is made.
- 3) All ports are marked as shown in paragraph 1 and other than those connected to Telecommunications Networks, may only have equipment complying with BS6301 connected to them.
- 4) This card is approved for direct connection as the following port types:-
2 wire connections: - Versions DTE90C, DTE91C, DTE92C and DTE93C only
A-law coding, VF only:
3BSX PSTN access private links, PSN speech, VF only
6AX Private network links, no PSTN traffic, VF only
A-law coding, with E & M signalling;
3BS PSTN access private links, PSN speech
6A Private network links, no PSTN traffic
ADPCM coding, with E & M signalling:
3BS PSTN access private links, PSN speech
6A Private network links, no PSTN traffic
4 wire connections: - Versions DTE90C, DTE91C, DTE92C and DTE93C only
A-law coding, VF only:
3CSX PSTN access private links, PSN speech, VF only
6BX Private network links, no PSTN traffic, VF only
A-law coding, with E & M signalling:
3CS PSTN access private links, PSN speech
6B Private network links no PSTN traffic
ADPCM coding, with E & M signalling:
3CS PSTN access private links, PSN speech
6B Private network links, no PSTN traffic cont'd.
- 5) This card is approved for connection via the isolation barrier DT290 as the following port types:
2 Wire connections:- Versions DTE90C, DTE91C, DTE92C and DTE93C only.
A-law coding with E & M signalling:
2BS PSTN access leased lines, PSN speech
5A Private network leased lines, no PSTN traffic
ADPCM coding with E & M signalling:
2BS PSTN access leased lines, PSN speech
5A Private network leased lines, no PSTN traffic
4 Wire connections:- Versions DTE90C, DTE91C, DTE92C and DTE93C only.
A law coding with E&M signalling:
2CS PSTN access leased lines, PSN speech
5B Private network leased lines, no traffic
ADPCM coding, with E & M signalling:
2CS PSTN access leased lines, PSN speech
5B Private network leased lines, no PSTN traffic.

Contents

1. General Description	7
2. Operation	8
3. Specifications	9
3.1 VF Characteristics	9
3.2 VF Levels	10
3.3 VF Impedance	10
3.4 VF Frequency Response	10
3.5 Idle Channel Noise	10
3.6 Power Requirements	10
3.7 Signalling DTE 91/91C and DTE 93/93C	10
4. Network Planning	11
5. Configuration	12
5.1 Timeslot Allocation	12
5.2 VF Level settings	13
6. Signalling Characteristics	15
7. Link and Switch Settings	16
7.1 Daughter Board Switch Settings	17
7.2 Status Ports	17
7.3 Control Ports	17
8. Connections	18

8 Channel 2/4 Wire ADPCM Card

1. General Description

This channel card provides eight 2 or 4 wire VF interfaces on a mother board DT516, with the option to plug in a single daughter board which will provide various options of E&M signalling, 32kbit/s ADPCM, and 16kbit/s ADPCM.

The following versions of the card are available:-

DTE90 8 channel 2/4 wire 64kbit/s VF card.

DTE91 8 channel 2/4 wire 64kbit/s VF/E&M card.

DTE92 8 channel 2/4 wire 32kbit/s ADPCM card 600 Ω impedance.

DTE93 8 channel 2/4 wire 32kbit/s ADPCM/E&M card.

DTE94 8 channel 2/4 wire 16kbit/s ADPCM card .

DTE90C 8 channel 2/4 wire 64kbit/s VF card.

DTE91C 8 channel 2/4 wire 64kbit/s VF/E&M card.

DTE92C 8 channel 2/4 wire 32kbit/s ADPCM card 600 Ω 4W impedance.

DTE93C 8 channel 2/4 wire 32kbit/s ADPCM/E&M card 2W Complex Z.

DTE94C 8 channel 2/4 wire 16kbit/s ADPCM card.

2. Operation

1) DTE90/90C (64kbit/s)

Each circuit drops digitally encoded voice data at 64k from selected backplane timeslots and converts it to an analogue VF output.

Analogue VF input signals are converted to digitally encoded voice data and are inserted into the selected backplane timeslots.

2) DTE91/91C (64kbit/s plus E&M).

Provides 64k voice translation as the DTE90 but additionally supports E&M signalling

Channel Associated Signalling (CAS) data is dropped from the incoming timeslot 16 and used to operate the 'E' wire signalling relays. A signalling detector is used to convert the analog 'M' wire signalling input into a digital code, which is inserted into the outgoing timeslot 16.

3) DTE92/92C (32kbit/s ADPCM).

Two analogue VF input signals are converted into digitally encoded voice data, compressed via ADPCM at 32k, and inserted into a single selected timeslot.

ADPCM compressed digital data at 32k in a selected timeslot is dropped and converted into two analogue VF outputs.

The 32kbit/s ADPCM compression conforms to CCITT recommendation G721 blue book.

4) DTE93/93C (32kbit/s ADPCM plus E&M).

Provides the same voice translation as the DTE92 but additionally supports E&M signalling.

The signalling detectors of the two 32kbit/s circuits convert the analog 'M' wire signalling inputs into a digital form, combine and insert them into timeslot 16.

Encoded signalling data in timeslot 16 is dropped and decoded to drive the 'E' wire signalling relays of the two selected circuits.

5) DTE94/94C (16kbit/s ADPCM).

Analogue VF input signals on 4 channels are converted into digital data, compressed via ADPCM at 16k and inserted into a single selected timeslot.

ADPCM compressed digital data at 16k is dropped from a selected timeslot and converted into 4 analogue VF outputs.

Some limited E&M signalling can be provided - contact Case Technology for details.

3. Specifications

3.1 VF Characteristics

DTE90/90C and DTE91/91C.

The VF inputs are digitally encoded/decoded using the A-law (CCITT recommendation G711).

DTE92/92C, DTE93/93C and DTE94/94C.

The VF inputs are digitally encoded using ADPCM variants in accordance with CCITT recommendation G721.

Performance specification for all versions meets or exceeds:-

CCITT Rec. G712 and G714 for 4 Wire Systems.

CCITT Rec. G713 and G715 for 2 Wire Systems

and the relevant sections of OFTEL OTR001 for both 2 and 4 wire circuits except for absolute group delay as follows:-

G712	4 wire delay	A to A	640ms (600ms)
G714	4 wire delay	D to A	380ms (240ms)
		A to A	640ms (600ms)
G715	2 wire delay	D to A	390ms (300ms)

Figures in brackets are CCITT specification.

3.2 VF Levels

Software selectable in 1dB steps.

Tx: + 2.0 dBm to - 5.0 dBm

Rx: + 2.0 dBm to - 5.0 dBm

The isolation barrier DT290 if used, has an insertion loss of 0.8dB.

3.3 VF Impedance

For DTE90 to 94 the input and output impedance's are 600 ohms balanced.

For DTE90C to 94C the input and output impedance's for four wire circuits are 600 ohms balanced. Two wire circuits are a complex impedance, balanced, as defined in BS6305 1982 fig 5.

3.4 VF Frequency Response

Reference 800 Hz Transmit to Receive via one PCM link.

300Hz - 3,000 Hz \pm 0.5 dB

3,000 Hz - 3,400 Hz + 0.5/- 1.8 dB

3.5 Idle Channel Noise

< 65 dBm0 Weighted

3.6 Power Requirements

DTE90/90C: 4 Watts per card

DTE91/91C, 92/92C, 93/93C, 94/94C: 6 Watts per card

3.7 Signalling DTE 91/91C and DTE 93/93C

'E' + 'M' signalling is provided via Timeslot 16.

'M' - lead (Tx) Earth operation only

'E' - lead (Rx) busy condition Earth or Battery by link selection. Battery operation of the 'E' lead is only possible in a DC powered chassis or if an external DC supply is connected to an AC powered chassis.

4. Network Planning

The Code of Practice for the Design of Private Telecommunications Networks requires that delay, gain and quantisation distortion for a complete branch network are within certain limits. The following information is provided to assist with network planning.

Delay

The delays introduced by the channel card are:-

A-law coding	Backplane to VF: 210 μ s
	VF to backplane: 270 μ s
ADPCM coding	Backplane to VF: 335 μ s
	VF to backplane: 395 μ s

These delays must be added to those quoted in the handbook for the relevant multiplexer chassis.

Gain

The relative level of the VF input port is selectable between +2dBr and -5dBr.

The relative level of the VF output port is selectable between +2dBr and -5dBr.

The relative level of the PCM port is 0dBr.

Quantisation Distortion

For 64k A-law operation the quantisation distortion for a VF to VF connection is 1 qdu.

For 32kbit/s ADPCM operation the quantisation distortion for a VF to VF connection is 3.5 qdu.

5. Configuration

5.1 Timeslot Allocation

8 V.F. channels are grouped as 4 pairs, 1a and 1b through to 4a and 4b.

a) 8 channel working at 64kbit/s:

The following timeslot allocation rules apply.

- (i) Two sequential timeslots that do not cross frame boundaries may be allocated to circuits 1 to 4 in any order.
- (ii) Circuit 1 will apply to VF channels 1a and 1b.
Circuit 2 will apply to VF channels 2a and 2b and so on.
- (iii) The first timeslot allocated to a circuit refers to VF channel 'a', the second timeslot to VF channel 'b'
- (iv) VF channel 'b' cannot be accessed without access to VF channel 'a' first.
- (v) VF channel 'b' may be inhibited by not assigning the second timeslot.

b) 8 channel working at 32kbit/s ADPCM:

The following timeslot allocation rules apply.

- (i) Timeslot allocation is restricted to four sequential timeslots that do not cross frame boundaries.
- (ii) The first timeslot allocated must be assigned to circuit 1 and applies to VF channels 1a and 1b. Similarly the second, third and fourth timeslots to VF channels 2, 3 and 4 respectively.
- (iii) The first four bits of a timeslot are associated with VF channel 'a' and the last four bits to VF channel 'b'.
- (iv) VF channels must be de-allocated as pairs and from circuit 4 towards circuit 1, i.e. if only 3 ADPCM timeslots required for six VF channels, then circuits 1, 2 and 3 must be used.

c) 8 channel working at 16kbit/s ADPCM:

The following timeslot allocation rules apply.

- (i) Timeslot allocation is restricted to two sequential timeslots that do not cross frame boundaries.
- (ii) The first allocated timeslot must be assigned to circuit 1 and applies to VF channels 1a, 1b, 2a and 2b. The second allocated timeslot is assigned to circuit 2 and applies to VF channels 3a, 3b, 4a and 4b.
- (iii) The first 2 bits of a timeslot is associated with V.F. channel 1a(3a), the 3rd and 4th bits to VF channel 1b(3b), the 5th and 6th bits to VF channel 2a(4a) and the last two bits to V.F. channel 2b(4b).
- (iv) If only 1 timeslot is allocated then it must be assigned to circuit 1 to give VF channels 1a, 1b, 2a and 2b.

5.2 VF Level settings

The gain of each VF channel is controlled by the multiplexer 'TS Control' facility.

The control byte is 12H for normal operation.

The control byte has the function as shown in Figure 1-1.

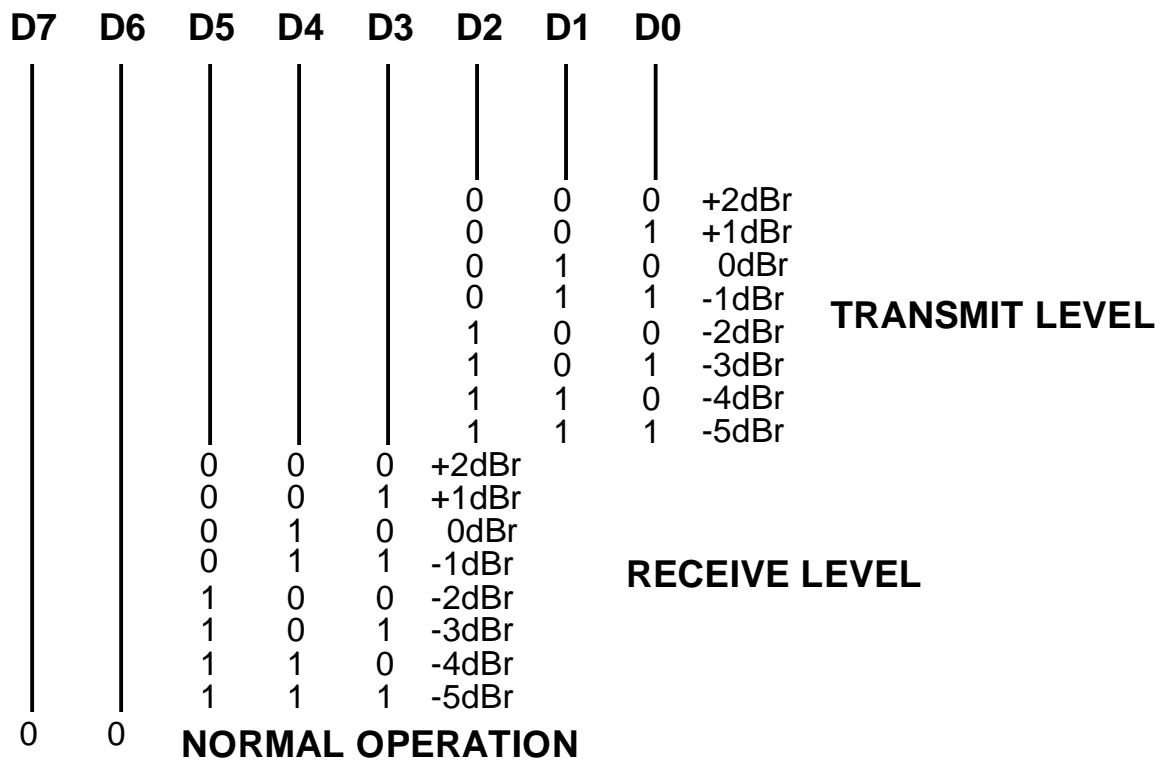


Figure 1-1 TS Control Values

Notes:

- 1 For 32kbit/s ADPCM operation:
One timeslot control byte controls 2 VF channels.
i.e. 1a and 1b, or 2a and 2b, or 3a and 3b, or 4a and 4b.
- 2 For 16kbit/s ADPCM operation:
One timeslot control byte controls 4 VF channels.
i.e. 1a, 1b, 2a and 2b or 3a, 3b, 4a and 4b.

6. Signalling Characteristics

1) INPUT 'M' LEAD.

Earth ON (busy condition): Up to 1500 ohms in parallel with a 1 μ F capacitor from input to earth.

Earth OFF (idle condition): Resistance of 400k ohms in parallel with a 1 μ F capacitor from input to earth.

NOTE: The maximum continuous voltage applied to the 'M' wire inputs should not exceed -28V/+4V.

2) OUTPUT 'E' LEAD.

Earth ON (busy condition): 1200 ohms in parallel with a 1 μ F from output to earth.

Earth OFF (idle condition): 1 μ F capacitor from output to earth.

NOTE: If the card is operating in a battery powered chassis, or a mains chassis with an external battery connected, setting LK3 to position 2-3 will set the 'E' output to -48V instead of earth.

3) TS16 CAS Signalling codes

a) 8 Channel VF Mode

TS16 output codes, per circuit, for 'M' lead input connection state, are as follows:-

	a	b	c	d
IDLE (earth off)	1	1	0	1
BUSY (earth on)	0	1	0	1

Detection of TS16 Busy code sets the 'E' lead output to BUSY (earth on), any other code sets IDLE (earth off).

NOTE: BUSY code detection/generation, and IDLE code generation are programmable by a change of mother board IC.

b) 32kbit/s ADPCM Mode

Reference CCITT recommendation G761.

TS16 output codes, per circuit pair (M1, M2), for 'M' lead input connection state are as follows:-

	a	b	c	d
M1	1		M2	1

M1, M2 = 0 BUSY (earth on), 1 IDLE (earth off)

NOTE: M1 refers to VF 'a' channel signalling: M2 refers to V.F. 'b' channel signalling. 'E' lead connection status is based only on the state of the appropriate circuit bit, M1 or M2, i.e. bits b and d are ignored.

7. Link and Switch Settings

Link 34 Position. 1-2 earth 'E' output signalling
 Position. 2-3 battery 'E' output signalling

Links 2 to 33 Position. 1-2 4 wire operation
 Position. 2-3 2 wire operation

There are 4 links per circuit as per the following table:-

CCT	LINKS
1A	13, 14, 29, 30
1B	9, 10, 25, 26
2A	5, 6, 21, 22
2B	2, 17, 18, 33
3A	15, 16, 31, 32
3B	11, 12, 27, 28
4A	7, 8, 23, 24
4B	3, 4, 19, 20

7.1 Daughter Board Switch Settings

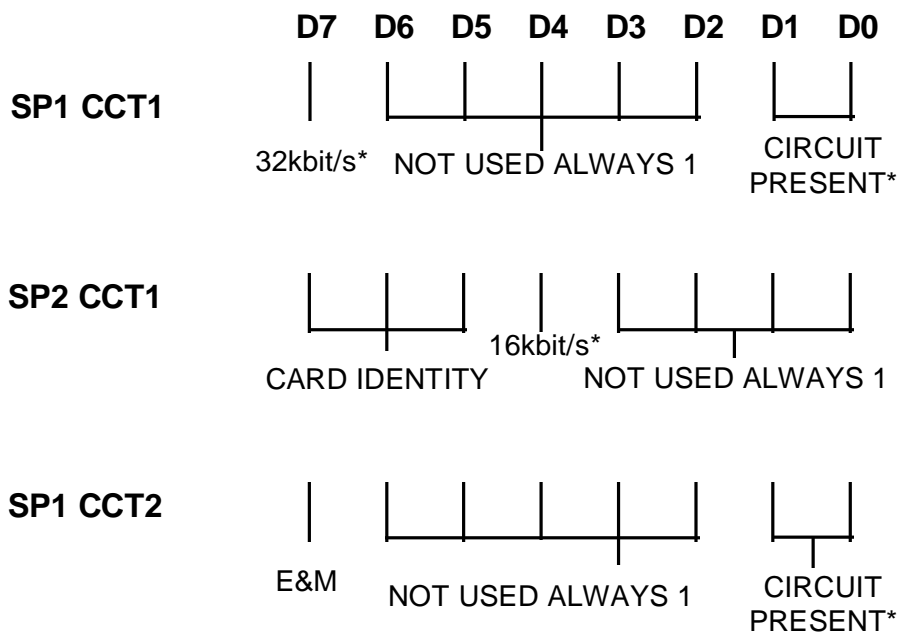
Referenced to silkscreen

	S1	S2	S3	S4	S5	S6
DTE91 (VF + E+M)	X	X	X	X	ON	X
DTE92 (32kbit/s)	32	16/32	OFF	ON	OFF	ON
DTE93 (32kbit/s+ E+M)	32	16/32	OFF	ON	ON	ON
DTE94 (16kbit/s)	16	16/32	ON	OFF	OFF	OFF

X= NOT FITTED

7.2 Status Ports

Status Port (SP) 1 and 2 for circuit 1 and Status Port 1 for circuit 2 are used on this card.



* 0 when card is present or active.

7.3 Control Ports

The Control Ports are not used by this card.

8. Connections

Connections to the VF and signalling lines are via the DIN 41612 I/O connectors on the back panel. The connections are as follows:-

32a (50) (CCT.2b) RxB	32c (25) (CCT.4b) RxB
31a (49) (CCT.2b) RxA	31c (24) (CCT.4b) RxA
30a (48) (CCT.2b) E-Lead	30c (23) (CCT.4b) E-Lead
29a (47) (CCT.2b) TxA (2 wire TX/Rx)	29c (22) (CCT.4b) TxA (2 wire TX/Rx)
28a (46) (CCT.2b) TxB (2 wire Tx/Rx)	28c (21) (CCT.4b) TxB (2 wire Tx/Rx)
27a (45) (CCT.2b) M-Lead	27c (20) (CCT.4b) M-Lead
26a Earth	26c 0V
25a *	25c *
24a (44) (CCT.2a) RxA	24c (19) (CCT.4a) RxA
23a (43) (CCT.2a) RxB	23c (18) (CCT.4a) RxB
22a (42) (CCT.2a) E-Lead	22c (17) (CCT.4a) E-Lead
21a (41) (CCT.2a) TxA (2 wire Tx/Rx)	21c (16) (CCT.4a) TxA (2 wire TX/Rx)
20a (40) (CCT.2a) TxB (2 wire Tx/Rx)	20c (15) (CCT.4a) Tx B (2 wire Tx/Rx)
19a (39) (CCT.2a) M-Lead	19c (14) (CCT.4a) M-Lead
18a Earth	18c 0V
17a *	17c *
16a (38) (CCT.1b) RxA	16c (13) (CCT.3b) RxA
15a (37) (CCT.1b) RxB	15c (12) (CCT.3b) RxB
14a (36) (CCT.1b) E-Lead	14c (11) (CCT.3b) E-Lead
13a (35) (CCT.1b) TxA (2 wire Tx/Rx)	13c (10) (CCT.3b) TxA (2 wire TX/Rx)
12a (34) (CCT.1b) TxB (2 wire Tx/Rx)	12c (9) (CCT.3b) TxB (2 wire Tx/Rx)
11a (33) (CCT.1b) M-Lead	11c (8) (CCT.3b) M-Lead
10a Earth	10c 0V
9a *	9c *
8a (32) (CCT.1a) RxA	8c (7) (CCT.3a) RxA
7a (31) (CCT.1a) RxB	7c (6) (CCT.3a) RxB
6a (30) (CCT.1a) E-Lead	6c (5) (CCT.3a) E-Lead
5a (29) (CCT.1a) TxA (2 wire Tx/Rx)	5c (4) (CCT.3a) TxA (2 wire TX/Rx)
4a (28) (CCT.1a) TxB (2 wire Tx/Rx)	4c (3) (CCT.3a) TxB (2 wire Tx/Rx)
3a (27) (CCT.1a) M-Lead	3c (2) (CCT.3a) M-Lead
2a (26) Earth	2c (1) 0V
1a *	1c *

* Bussed backplane signals - no connection should be made to these pins.

TxA/TxB and RxA/RxB refer to the balanced pairs in each case.

When viewed from the rear of the chassis, pin 1a is the bottom left hand pin of the connector. Pin connections in brackets refer to those on the Amphenol 50 pin socket used on the DT 280 adapter or on the Case Technology 2100 multiplexer.