

# **64k Sub-Multiplex Card Operation Manual**

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## STATUTORY NOTICES

### APPROVAL

The card is approved for indirect connection to Telecommunications Systems under the General Approval Number NS/G/1234/J/100003. The card does not contain safety isolation barriers, and any apparatus connected to it must conform with the safety requirements of the General Approval.

The safety status of the interface is SELV.



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

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All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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# Quad 2 Wire Exchange Interface Card

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## 1. Description

The DTE85 64k Sub-Multiplex card uses a basic DT550 card fitted with DT940 firmware. The card may be used in the Cray Communications range of 2000 and 3000 multiplexers.

The DTE85 provides 6 full duplex V.24/V.28 independent circuits time division multiplexed (TDM) on to one 64kbit/s timeslot. Signalling circuits supported are RTS, RFS, DCD on all ports, and DTR and DSR on two ports only. One V.28 clock input and one V.28 clock output provide for two different clocking modes in synchronous operation, while the data format in asynchronous operation can be 7 or 8 data bits with 2 stop bits.

Six data rates are supported 19200, 9600, 4800, 2400, 1200 and 600bit/s however the maximum aggregate data rate limit of 57.6kbit/s dictates that only three ports can operate at 19200bit/s. The remaining 10% of the 64kbit/s bandwidth is used for framing and signalling.

Status LEDs are provided to monitor the V.28 signals and to indicate any alarm conditions.

## 2. Specifications

Meets CCITT recommendations V.24 with V.28 electrical levels.

Circuits supported:-

103, 104, 105, 106, 109, 115, 113, 102 on all ports  
107, 108 ports 1 & 2 only.

## **Data Rates**

600	bit/s
1200	bit/s
2400	bit/s
4800	bit/s
9600	bit/s
19200	bit/s

The maximum combined aggregate data rate for all circuits is 57.6kbit/s, (6.4kbit/s is used for framing and signalling).

## **Delays**

The maximum end to end delays contributed by this card are as follows:

### **Asynchronous Data**

Max delay             $6\text{ms} + (20 \div \text{the data rate in kbit/s})$ .  
e.g. 7ms @ 19.2kbit/s,    40ms @ 600bit/s

### **Synchronous Data**

Max delay             $88 \div \text{the data rate in kbit/s}$ .  
e.g. 4.6ms @ 19.2kbit/s,    147ms @ 600bit/s

## **Signalling**

Max delay 7.5ms

## **Power Requirements**

6.5 Watts per card.

### **3. Operation**

The 64kbit/s Sub Mux data card generates its own TDM frame structure in order to transfer the incoming V.24 data across the PCM. This frame structure will be referred to as the 'Sub-mux frame structure' in order to differentiate it from the PCM frame structure. The sub-mux frame structure also contains a communication channel, which is used to transfer configuration data from the local unit to the remote unit. When enabled, the local and remote configurations are compared to check for compatibility in the end to end circuits, i.e. async and sync ports are not connected together and end to end data rates are the same.

#### **3.1 Signalling**

Incoming signalling is sampled every 2.5ms and is inserted into the sub-mux frame structure. At the remote sub-mux card, the signalling data is dropped from the PCM and simultaneously written out to all ports.

Each port supports an RTS signalling input. Conditions on this input appear as DCD at the remote end and locally as RFS. An optional delay can be applied to the RFS output so that RFS will be asserted either nominally 35 or 50ms after RTS. This delay will apply to all circuits. Ports 1 and 2 additionally support DSR and DTR.

#### **3.2 Synchronous Data**

When the card is configured, mode switches determine which clocks are to be used to sample transmit (incoming) data and clock out receive (outgoing) data at the channel interface. Transmit data is assembled into 8 bit words before being entered into a buffer store, which is able to accommodate for a minimum of 8 bits of line timing jitter. The data is then removed from the buffer and inserted into the sub-mux frame structure which is carried in the appropriate timeslot of the PCM. At the remote sub-mux card, data is dropped from this timeslot, decoded and inserted into a second buffer store before being presented as receive data at the channel interface.

#### **3.3 Synchronous Clocking Modes**

In synchronous mode, a port can operate in two clocking modes: Synchronous (DCE) and Modem. In 'Sync' mode, Transmit and Receive data are both clocked using the sub-mux internal clock. This clock is available on the 'RC' V.28 output.

When 'Modem' mode is selected, Receive data is clocked out using the internal clock, but Transmit data is sampled using the external clock. The external clock must be present on the 'TC' V.28 input.

The Receive clock output is intended for connection to either pin 15 or 17 at the V.24 interface. If connection is made to two receivers the level will be outside CCITT recommendations for V.28 signals.

### **3.4 Asynchronous Data**

Data must be converted to a synchronous format before being transferred across the PCM. This is achieved by using the fact that start and stop bits do not have to be transferred along with the data. Any incoming data is stored over a two Sub Mux frame period. During the next two Sub Mux frames, the stored byte count followed by the data is inserted into the appropriate timeslot, while further incoming data is stored. At the remote end the byte count is detected and any following data is presented as receive output data with start and stop bits added.

By storing the incoming data over a two Sub Mux frame period, asynchronous data incurs a 5ms delay before being inserted into the PCM.

The format for the asynchronous data during transmission is fixed at 8 Bits, 2 Stop bits, No parity. This allows user data of either 7 bits plus parity, or 8 bits no parity to be carried. Two stop bits must always be included.

### **3.5 Sub Mux Frame Sync Loss**

If the Sub Mux card loses frame sync, e.g. due to PCM failure, the following actions will result :-

**Signalling** - All signalling outputs are immediately set to the 'off' state.

**Synchronous Data** - The output data will be forced to '1'.

**Asynchronous Data** - After data already stored in the internal buffers has been transmitted, no further data will be sent.

### 3.6 Test Loops

The Sub Mux ports can be looped in both directions simultaneously according to CCITT recommendation X.150 types 3c and 2b.

All six ports can be looped simultaneously by using the 'Circuit loop' option in the Multiplexer control software. Individual ports can be looped using the 'Port loop' available on Control port 2.

When any port is looped the red Alarm/Loop LED will be lit, and the status LEDs will cease to function.

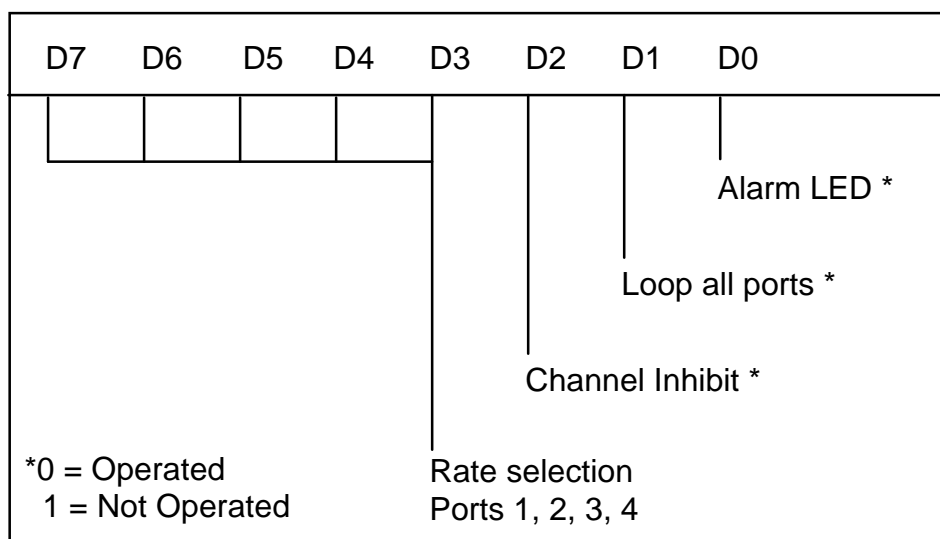
### 3.7 Test Access Connector

The test access connector on the front of the card is for manufacturing tests purposes only.

## 4.0 Control Port Functions

Both Control Ports 1 and 2 are used by this card. The control bytes are set up by the multiplexer software by modifying the 'Circuit Controls'.

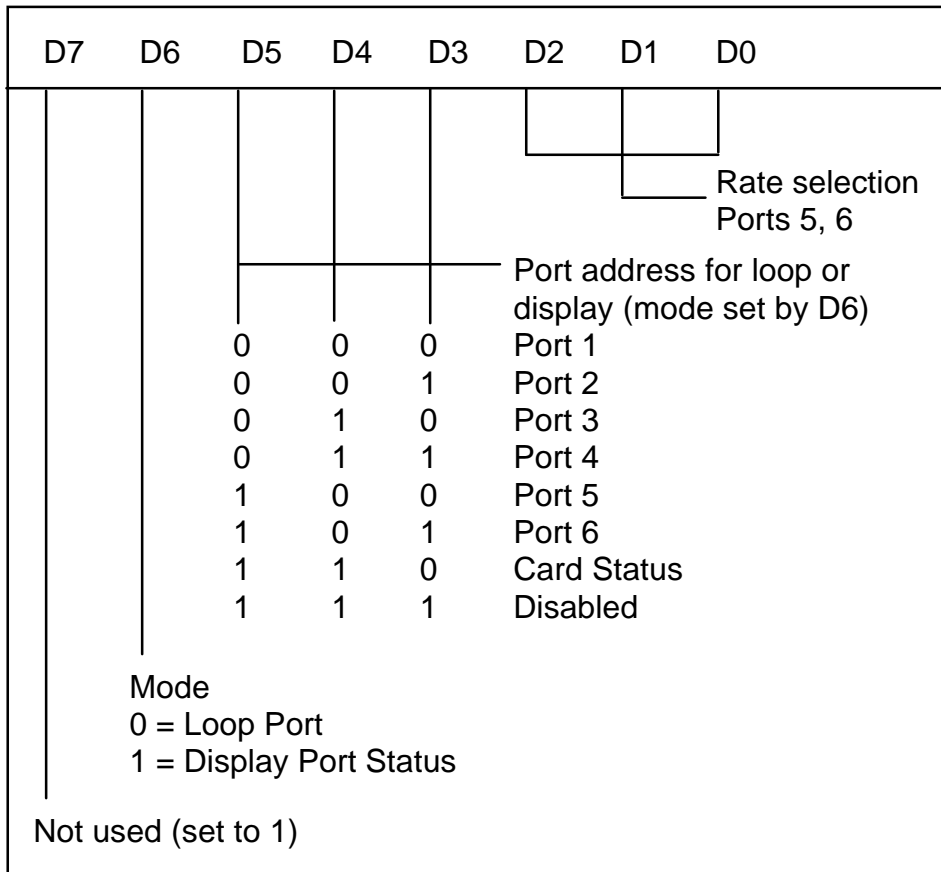
### Control Port 1



**Control Port 1 settings**

## Control Port 2

The 'Port Address' on control port 2 can be used to either apply an 'individual port loop', or to display the status of a port or any sub-mux active faults on status port 2, depending on the setting of the mode bit.



### Control Port 2 settings

## Data Rate Options

The following data rate options are available:

For Ports 1 to 4

CODE	PORT 1	PORT 2	PORT 3	PORT 4
00000	19200	19200	-	-
00001	19200	9600	-	9600
00010	19200	9600	-	4800
00011	19200	9600	-	2400
00100	19200	4800	-	4800
00101	19200	4800	-	2400
00110	19200	2400	-	2400
00111	19200	1200	-	1200
01000	19200	1200	-	600
01001	9600	9600	9600	9600
01010	9600	9600	4800	9600
01011	9600	9600	2400	9600
01100	9600	9600	1200	9600
01101	9600	9600	4800	4800
01110	9600	9600	2400	4800
01111	9600	9600	2400	2400
10000	9600	4800	4800	4800
10001	9600	4800	2400	4800
10010	9600	4800	2400	2400
10011	9600	4800	600	1200
10100	9600	2400	2400	2400
10101	4800	4800	4800	4800
10110	4800	4800	2400	4800
10111	4800	4800	1200	4800
11000	4800	4800	2400	2400
11001	4800	2400	2400	2400
11010	4800	2400	600	1200
11011	2400	2400	2400	2400
11100	2400	1200	1200	1200
11101	1200	1200	1200	1200
11110	1200	1200	600	600
11111	600	600	600	600

For Ports 5 and 6:

Code	Port 5	Port 6
000	19200	-
001	9600	9600
010	4800	4800
011	2400	2400
100	1200	1200
101	600	600
110	9600	4800
111	4800	2400

## 5. Status Port Facilities

The status bytes are monitored from within the multiplexer control software. \*All signals are active low. 0 = Operated or alarm condition.

### Status Port 1

D7	D6	D5	D4	D3	D2	D1	D0
Slip Port Address							Card present
0	0	0					
0	0	1					Data Circuit
0	1	0					
0	1	1					Slip
1	0	0					Alarm 1 (Hardware Alarm)
1	1	1					Alarm 2 (Operation Alarm)

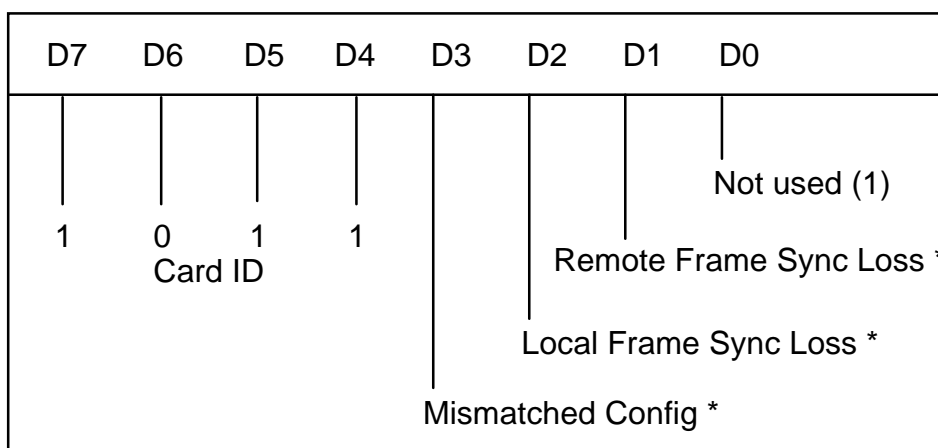
### Status Port 2

The status display options on status port 2 are selected by control port 2 bits D3, D4 and D5 to display either port status or card status.

Status Port 2 when display 'port status' is selected.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1				RTS *
							RFS *
							DCD *
							Mode 1=Sync 0=Async

Status Port 2 when display 'card status' is selected.



## 6. Alarm Conditions

**Slip:** Slip is only reported if a port in synchronous mode under or overflows either the input or output buffer, e.g. by excessive line timing jitter or clock loss. For the duration of the slip reporting period, 20 seconds, the address of the port that slipped will be displayed in status port 1. Should slips occur on more than one port, then a slip will be reported for each of the ports that have slipped.

**Alarm 1:** Alarm 1 is reported for a hardware fault, i.e. either self test fail or watchdog. The Sub Mux carries out a self test every time the card powers up or is reset by a watchdog pulse. Should a failure be detected, then Alarm 1 will be permanently reported and all the LEDs will either be permanently lit or flashing regularly depending on the type of failure detected. In the case of a watchdog failure, Alarm 1 will be reported for 20 seconds.

**Alarm 2:** Alarm 2 is reported for Sub Mux frame sync loss or a mismatch in end to end configurations if this feature is enabled by S2-4. Alarm 2 will be reported for at least five seconds.

## 7. Links

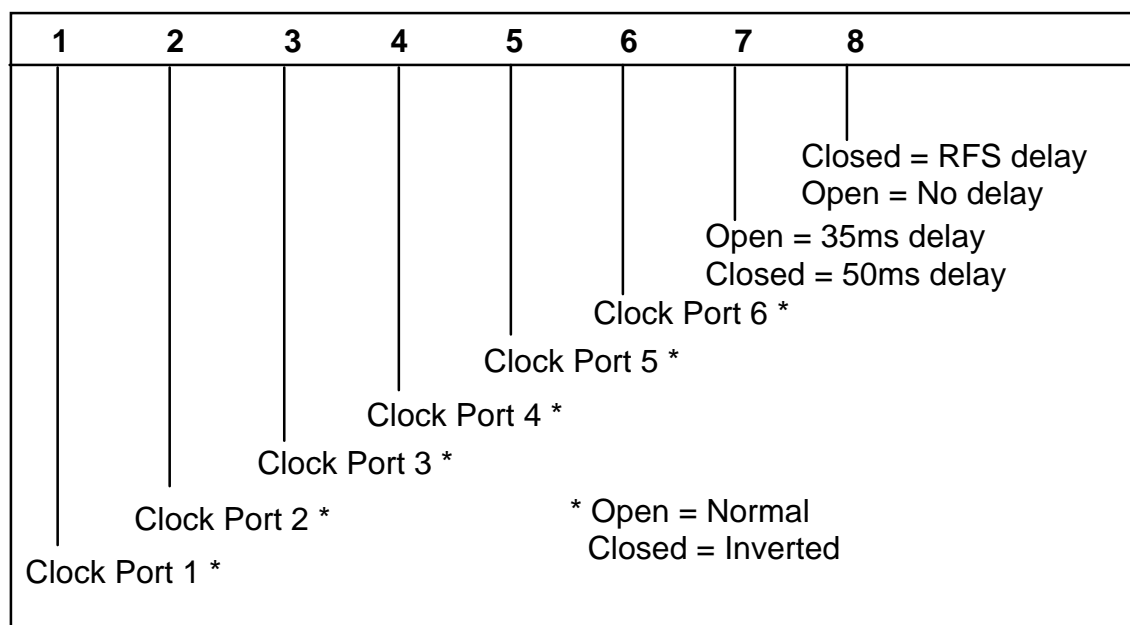
TL1 and LK2 are used for test purposes only and should be in position 1-2. LK1 must be in the NC position.

## 8. Switches

### Switch S1

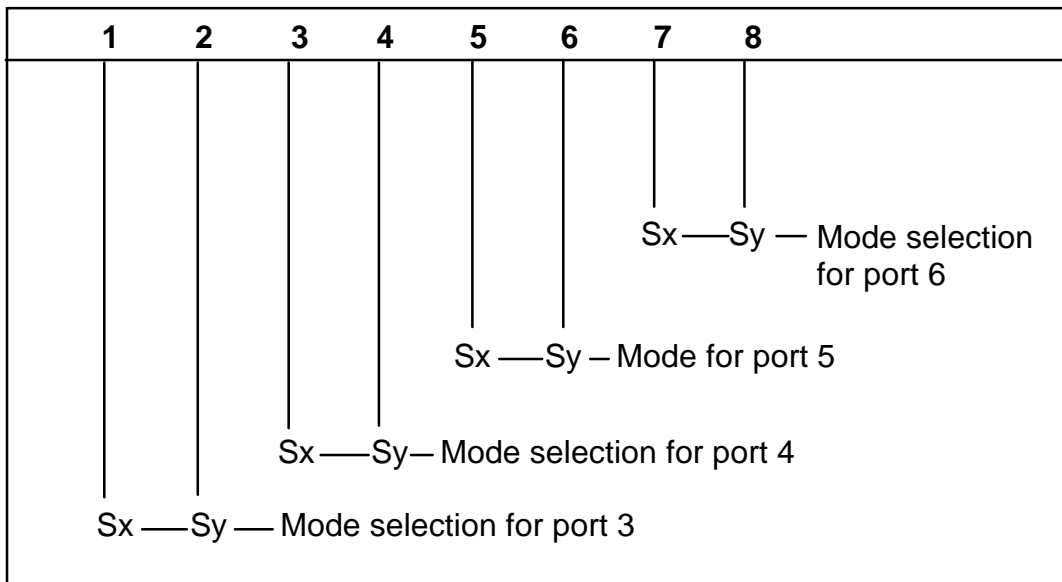
Receive Data (output) is clocked out on the rising edge of the V.28 clock selected, and the Transmit Data (input) is sampled on the falling edge. Under normal operating conditions this ensures that incoming data is sampled in the centre of each bit. If however long propagation delays mean that the incoming data is now changing close to the falling edge of the clock then S1 can be used to select sampling on the rising edge instead.

This switch also controls the delay imposed on the RFS (output) being active after the RTS (input) has been asserted.



**Switch S1 settings**





**Switch S3 settings**

## 9. LED Indicators

The red Alarm/Loop LED will always function irrespective of the setting of S2.

The LEDs can display the status of any one of the V.24/V.28 circuits or of the Sub Mux card itself as selected by switch S2. The LED display option switches may be changed at any time.

If the 'card status' option is selected then the LED display will help to identify any active faults affecting all ports.

If a 'port status' option is selected then the LED display will show the state of the control and data signals for the selected port. In this mode the LEDs will light if the relevant control line is active, or flash if data is present.

Port status will only be displayed when there is no Alarm/Loop condition.

LED	Port Status	Card Status
Green	Rx Data	Slip
Green	DCD	Mismatched configurations
Yellow	Tx Data	Local Frame Sync Loss
Yellow	RFS	Remote Frame Sync Loss
Yellow	RTS	Watchdog fail
Red	Alarm / Loop	

## 10. V.28 I/O Connections

Signal	CCITT Circuit	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	V24 Interface
TD	103	4c(3)	12c(9)	20c(15)	28c(21)	28b(46)	8b(32)	2
RD	104	8c(7)	16c(13)	24c(19)	32c(25)	32b(50)	21b(41)	3
RTS	105	3c(2)	11c(8)	19c(14)	27c(20)	24b(44)	7b(31)	4
RFS (CTS)	106	7c(6)	15c(12)	23c(18)	31c(24)	31b(49)	20b(40)	5
DSR	107	5b(29)	13b(35)	-	-	-	-	6
DTR	108	4b(28)	12b(34)	-	-	-	-	20
DCD	109	5c(4)	13c(10)	21c(16)	29c(22)	29b(47)	16b(38)	8
RCLK(o/p)	115	6c(5)	14c(11)	22c(17)	30c(23)	30b(48)	15b(37)	15 or 17
TCLK(i/p)*	113	3b(27)	11b(33)	19b(39)	27b(45)	23b(43)	14b(36)	24
SG	102	2c(1)	10c -	18c -	26c -	22b(42)	6b(30)	7

Earth from the multiplexer backplane is on 2b, 10b, 18b and 26b.

\* Tx Clock input when operating in Modem mode.

Note: Multiplexer connections are as viewed from the back of the chassis with pin 1a as the lower left hand pin.

Numbers in brackets refer to those on the 50 way Amphenol female connector on the Cray Communications 2100 multiplexer or on the universal I/O adapter DT280 if used.

