

Quad Co-directional Data Card Reference Manual

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STATUTORY NOTICES

APPROVALS

The Quad Co-directional card DT536 is approved for indirect connection to Telecommunication Systems under the General Approval Number NS/G/1234/J/100033.

This card does not contain safety isolation barriers, and any apparatus connected to it must conform with the safety requirements of the General Approval.

The safety status of the interface is SELV.

All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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Quad G.703 Co-directional Data Card

1. Description

The Quad G.703 Co-directional data card DT536, provides four independent 64kbit/s interface circuits, operating in four independent timeslots in a 2048kbit/s PCM stream.

2. Operation

The card provides four 64kbit/s interfaces as per CCITT recommendation (Red book) G.703 Co-directional working, i.e. the transmit and receive clocks are sent in the same direction as the transmit and receive data signals and on the same respective pair.

Two 8kHz clocks (8k1 and 8k2) are provided. They can be derived from any of the interface input data signals. These clocks may be used to synchronise the master timing within the multiplexer if desired.

3. Specifications

The Quad G.703 Co-directional card complies with the following CCITT specifications:-

1. G.703 64kbit/s Co-directional
2. X.150 Test Loops

Power Requirements

1.4 Watts per card

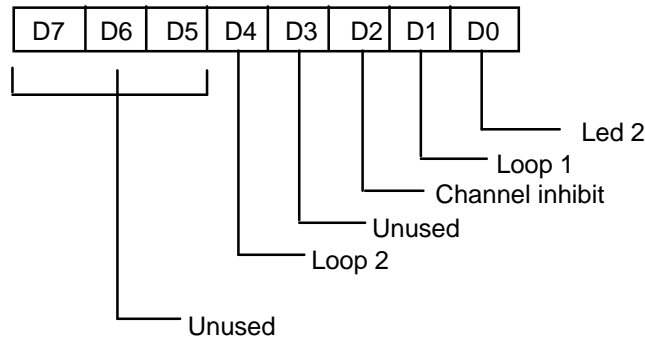
Delays

The delay contributed by the card in either direction is less than 400 μ s.

4. Control Port Functions

Only control port 1 is used by this card. The control byte is set up by the multiplexer software. All signals are active low.

The functions are as follows:

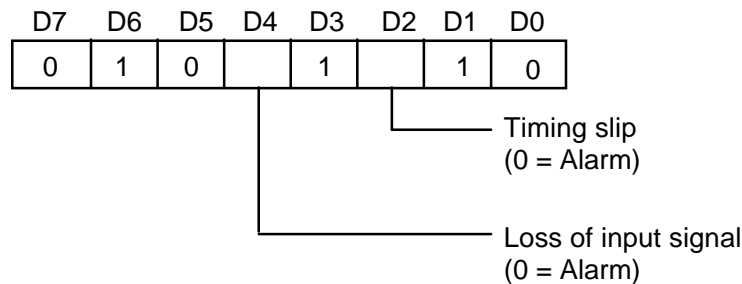


5. Status Port Facilities

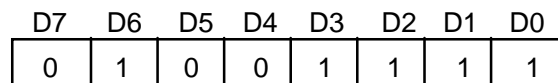
Status ports 1 and 2 are used by this card. The status byte can be monitored by the multiplexer maintenance software.

The signals are as follows:

Status port 1 (for each circuit):



Status port 2 (for each circuit):



Notes;

1. When channel inhibit is active, the timing slip and signal loss alarm reporting on status port 1 is inhibited.
2. When loop 2 is active, the timing slip alarm is not available and the signal loss alarm applies to the received looped data (See figure 1-1).

6. Fault Conditions

- a) The received data will be set to all 1's under the following conditions:
 - AIS received
 - local channel inhibit active

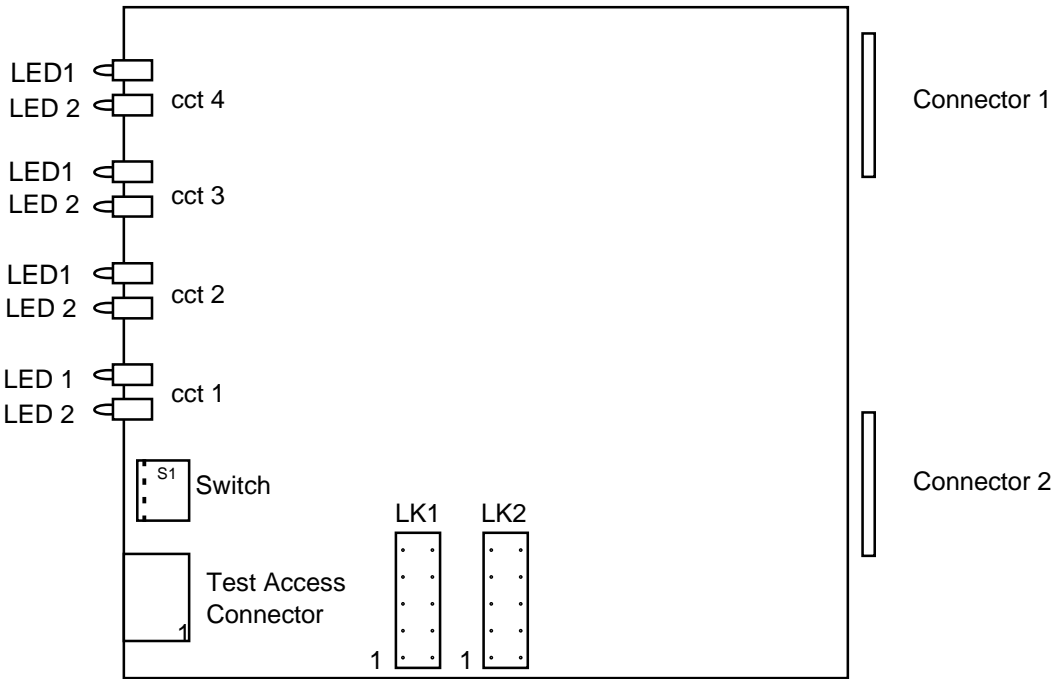
This does not apply if loop 1 is active.

- b) The transmit data will be set to all 1's under the following condition:
 - loss of input signal.

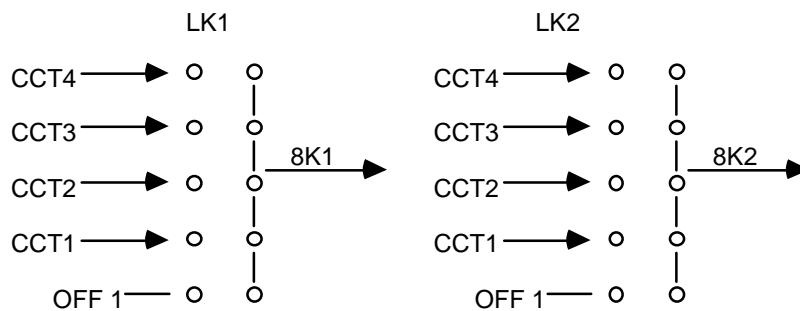
Note: Refer to Fig.1-1 for the position of receive and transmit data.

7. Links, LEDs, Switch and Test Access Connector

The following is a diagrammatical representation of the links, LEDs, switch and test access connector available on the card:



7.1 Links LK1 and LK2



The two 8kHz clocks (8k1 and 8k2) may be selected with LK1 and LK2.

Note: If channel inhibit or loop 2 is active or when a loss of input signal is detected, the 8kHz clock corresponding to this circuit is inhibited (low level).

7.2 LEDs

Two LEDs are provided for each circuit.

LED 1 lights when there is a loss of input signal or when loop 2 is active and a loss of the looped data occurs.

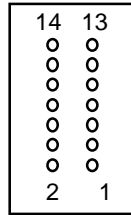
LED 2 lights when a loop is active or when a timing slip occurs. LED 2 is controlled by the control byte.

7.3 Test Access

Any of the four circuits transmit or receive analogue signals are available on pins 13 and 14 of the test access connector, 120 ohms balanced working.

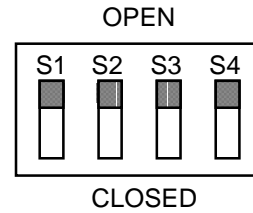
The required signal is selected by switches as follows:

Test access connector



Front view

Switch



S1	S2	S3	S4	Signal
C	C	C	X	TX1
O	C	C	X	TX2
C	O	C	X	TX3
O	O	C	X	TX4
C	C	O	X	RX1
O	C	O	X	RX2
C	O	O	X	RX3
O	O	O	X	RX4

C : Closed
 O : Open
 X : Closed or Open

TX1 : Transmit signal (CCT1)
 RX1 : Receive signal (CCT1)

8. Connections

The connections used for the G.703 Receive and Transmit signals on the chassis DIN 41612 connector are as follows:

Circuit	Function	Pin
CCT4	RXB	32b (50)
	RXA	32c (25)
	TXB	28b (46)
CCT3	TXA	28c (21)
	RXB	24b (44)
	RXA	24c (19)
CCT2	TXB	20b (40)
	TXA	20c (15)
	RXB	16b (38)
CCT1	RXA	16c (13)
	TXB	12b (34)
	TXA	12c (9)
CCT1	RXB	8b (32)
	RXA	8c (7)
	TXB	4b (28)
	TXA	4c (3)

Numbers in brackets refer to those on the 50 way amphenol connector used on the universal I/O adapter DT280.

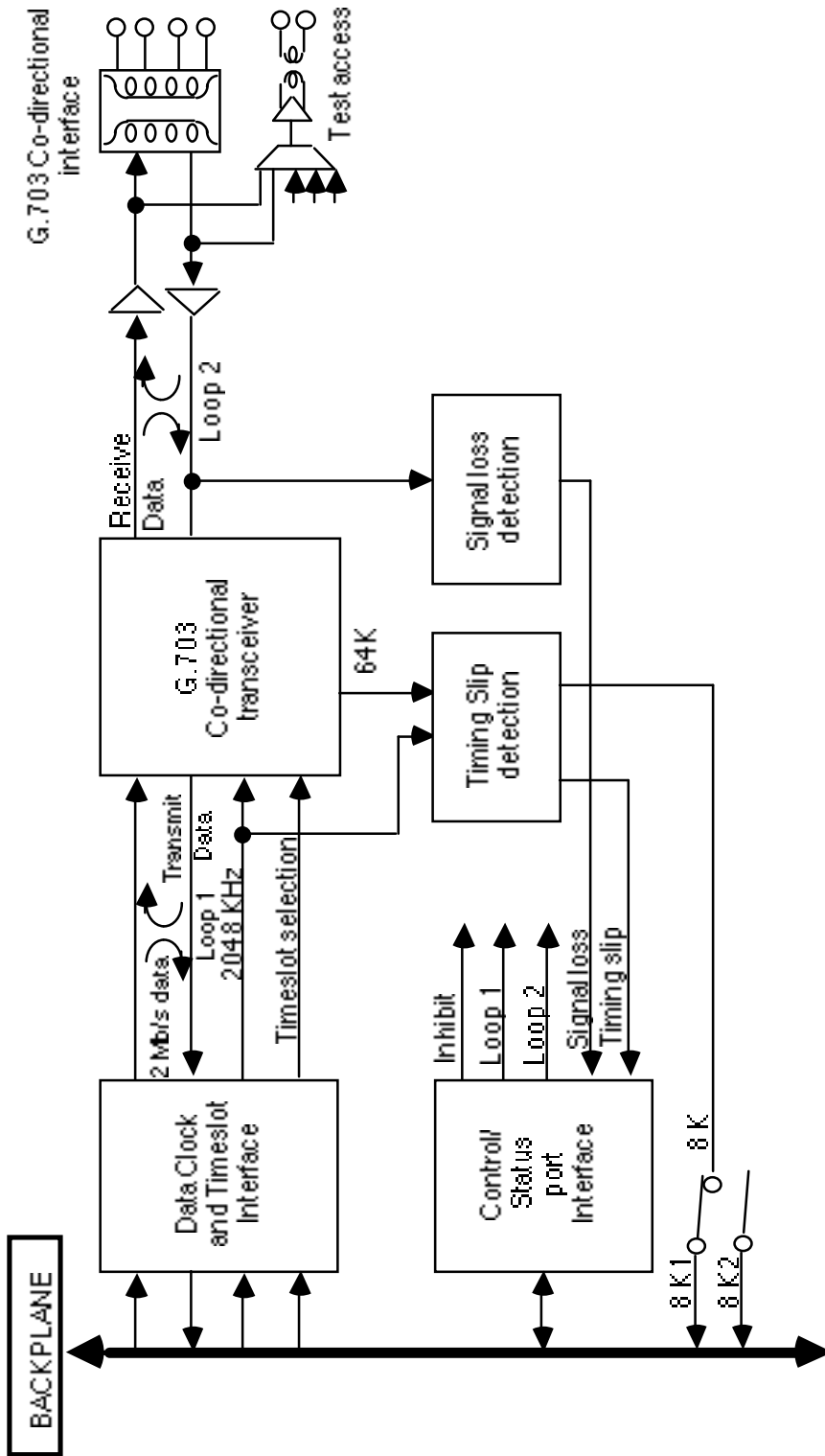


Figure 1-1 G.703 Co-directional Data Card Block Diagram (for one circuit)