

# **Dual V.24 Multipoint Card Reference Manual**

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## STATUTORY NOTICES

### APPROVALS

The Dual V.24 Multipoint Data Card DTE87 is approved for indirect connection to Telecommunications Systems under the General Approval Number NS/G/1234/J/100003. This card does not contain any isolation barriers, and any apparatus connected to it must conform to the requirements of the General Approval.

The safety status of the interface is SELV.



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

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All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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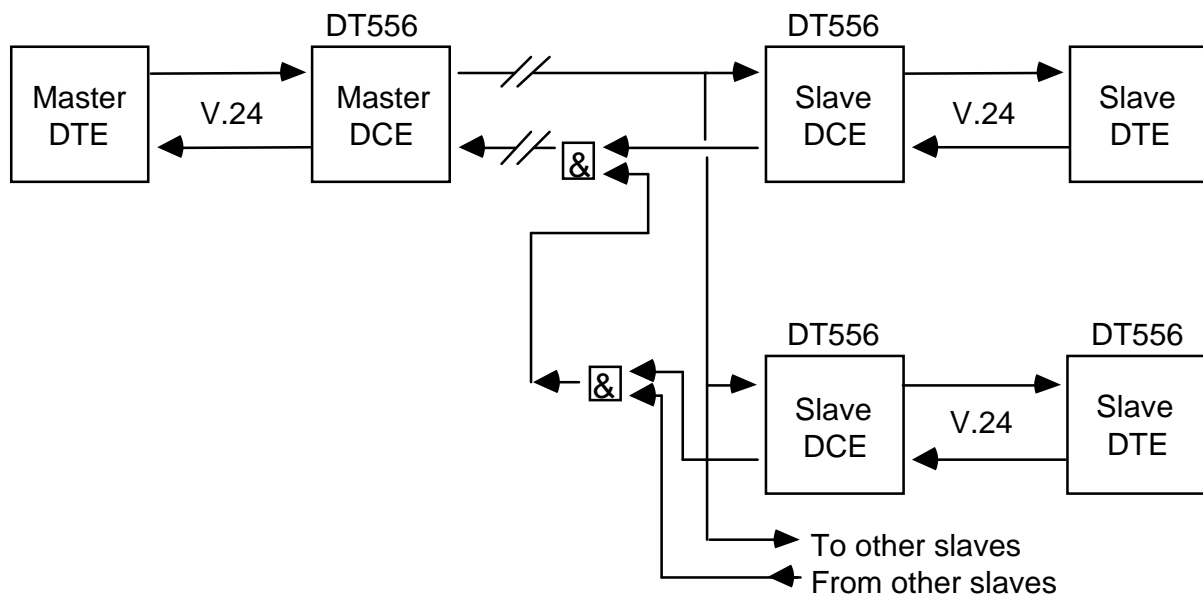
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## 1. Description

The Dual V.24 interface card provides for two full duplex V.24/V.28 independent data channels with user selectable baud rate to be multiplexed into one 64kbit/s timeslot, with a signalling method allowing point-to-point or point-to-multipoint operation. Signalling circuits supported are RTS, RFS, RLSD, DTR, and DSR.

The signalling method used, enables a central master to broadcast 600 - 19200bps asynchronous data in either or both of it's circuits to any number of remote slaves. If operating at 19200bps, only one channel should be active. The remote slaves can send asynchronous data to the master, one at a time, again using either or both of their circuits. The basic method of system connection is shown below:



### 1.1 Frame Structure

The Multipoint frame structure allows for highly effective multiplexing of the low speed data into the 64kbit/s timeslot. This is achieved by separating the eight bit PCM timeslot into two four bit channels, each carrying an independent framing structure in both directions.

This framing is transparent to the 2048kbit/s transmission system, and contains sync, signalling, and the V.24 data. The synchronisation method has been chosen to provide integrity and speed.

## **2. Basic Operation**

The 64kbps Centralised Multipoint Card can operate in one of two modes: Master or Slave. Both modes provide the same V.24 DCE interfaces to attached user DTE equipment. A framing structure is used to encode data received at the V.24 interfaces into a PCM timeslot, which, when coupled with the timeslot 'ANDing' facility of the host Multiplexer and control of the V.24 signalling inputs, enables multipoint operation. The received V.24 data must be 600, 1200, 2400, 4800, 9600 or 19200bps with two stop bits, but the system allows for independent selection of parity and the number of data bits.

If 19200bps operation is selected for one channel, the usage of the other channel is restricted to lower data rates, or disabled. Correct operation of this channel is not certain, as error free functioning is dependent upon the DTE data transfer rate used, not the baud rate. It is recommended that for guaranteed error free operation, the restricted channel is disabled using the control port settings.

The 64kbit/s timeslot may be used to carry 2 x 19200bps channels by utilising separate master and slave cards for each channel.

Although the data channels are independent, the master/slave mode of operation applies to both.

### **2.1 Master Operation**

Master operation is selected by a combination of Control Port and switch settings. The reason for two sources of mode configuration is to prevent inadvertent selection of master mode as only one master DTE87 can be present for one multipoint system. If two are configured, corruption of transmitted data results unless through control port selection, both masters occupy different channels - see Table 1-1.

If either of the settings for master operation are incorrect, the card will default to the slave mode.

The master continuously transmits the framing structure for both data channels into the assigned timeslot whether data requires to be transmitted or not. The master will also continuously attempt to extract the framing structure from the received assigned timeslot. If no timeslot is assigned, no data will be sent or received.

The master will only transmit data received from its V.24 ports when the appropriate V.24 signalling inputs are active (Refer to the master signalling section).

## **2.2 Slave Operation**

Slave operation is selected by a combination of Control Port and switch settings.

The slave will continuously attempt to extract the framing structure and any data from the received assigned timeslot, but will only transmit the framing structure for the relevant channel when the appropriate V.24 signalling input from the DTE is active (Refer to the slave signalling section). This ensures other slaves cannot transmit to the master when the V.24 signalling is inactive.

The system only allows for one slave to be transmitting to the master in each channel. If more than one slave attempts to transmit using the same channel at once, corruption and loss of data will result. However, it is possible for two slaves to transmit at the same time, as long as each uses a different channel. It is also possible for one slave to use both channels at once.

If no timeslot is assigned, no data will be sent or received.

## **3. Specifications**

Meets CCITT recommendations V.24 with V.28 electrical levels.

### **Circuits supported:-**

102, 103, 104, 105, 106, 107, 108, 109, 115 & 113.

### **Data rate:-**

600, 1200, 2400, 4800, 9600, 19200bps.

## Delays

The maximum end to end delays contributed by this card are as follows:

### Asynchronous data

Max. delay 3.5ms

### Signalling

Max. delay 3.5ms

### Typical Power Requirements

3.5 Watts per card

## 4. Basic Signalling

The following V.24 signals are utilised on the Centralised Multipoint Card:

CCITT	RS232	DTE	DCE	FUNCTION
102	AB	<—————>		Sig ground/com return
103	BA	—————>		TD transmit data
104	BB	<—————		RD receive data
105	CA	—————>		RTS request to send
106	CB	<—————		RFS ready for sending
107	CC	<—————		DSR data set ready
108	CD	—————>		DTR data terminal ready
109	CF	<—————		RLSD receive line signal detector

To ensure that data flow problems do not occur, all data sent by the DTE should contain two stop bits, and TD (Transmit Data) be held at '1' for a minimum of 20 clock periods before changing RTS. This equates to 32ms at 600bps, and 1ms at 19200bps, or two discardable characters. All V.24 data transmitted by the Multipoint card will contain one stop bit.

### 4.1 Master Signalling

Asynchronous data will only be accepted from the V.24 interfaces if both RTS and DTR inputs are active. The state of the RLSD signal indicates the status of the received PCM information for that channel: When active, it indicates that valid framing is being received from the slave. When inactive, it indicates that no slave is responding, or incorrect/no framing structure received.

The DSR signal is a local reflection of the DTR signal.

The RFS signal is a local reflection of the RTS signal, via an optional delay set on switch S1.

## **4.2 Slave Signalling**

Asynchronous data will only be accepted from the V.24 interfaces if both RTS and DTR inputs are active. The state of the RLSD signal indicates the status of the received PCM information for that channel: When active, it indicates the master multipoint card's RTS input is active. When inactive, it indicates the master multipoint card's RTS input is inactive, or incorrect/no framing structure received.

The RTS signal is used to control the slave's transmission of data into the PCM for that channel. When active, the slave commences to send the framing structure and any received V.24 data. When inactive, the slave transmits an all 1's code into the channel, allowing its use by other slaves.

The DSR signal is a local reflection of the DTR signal.

The RFS signal is a local reflection of the RTS signal, via an optional delay set on switch S1.

## **5. Test Loops**

The Multipoint card's ports can be looped in both directions simultaneously according to CCITT recommendation X.150 types 3c and 2b.

Both ports can be looped simultaneously by using the 'Circuit loop' option within the multiplexer maintenance control software.

It is not possible to loop just one of the ports.

When a loop is applied, the RED Alarm/Loop LED will be lit.

Looping of the ports is only recommended in a point-to-point configuration. Looping of a slave in a point-to-multipoint system will cause corruption and loss of data.

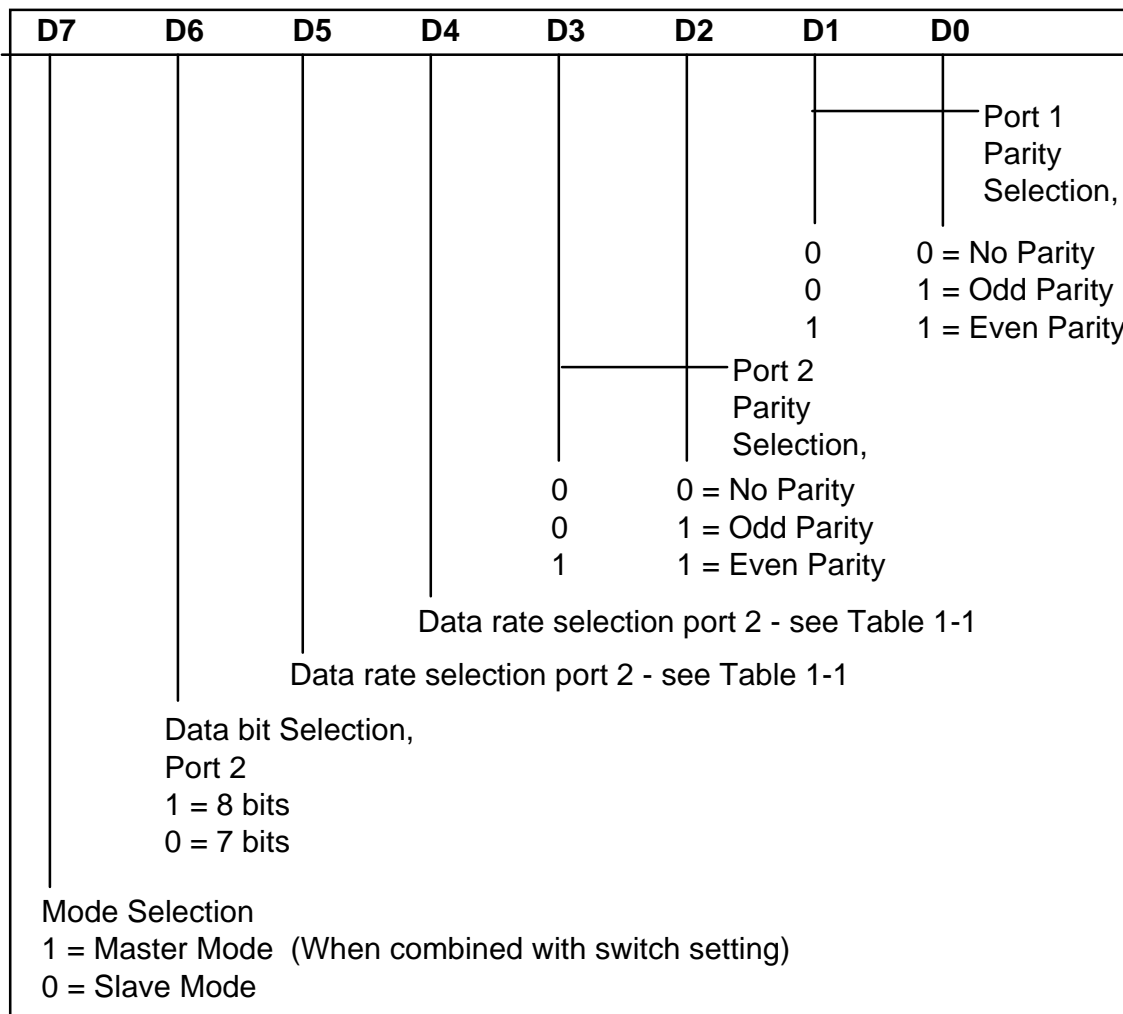
## 6. Control Port Functions

Both Control Ports 1 and 2 are used by this card. The control bytes are set up by the host multiplexer configuration software under 'Circuit controls'.

### Control Port 1

D7	D6	D5	D4	D3	D2	D1	D0
							Alarm LED*
						Loops Ports *	
					Channel Inhibit *		
				Data bit selection port 1 1 = 8 bits 0 = 7 bits			
			Data rate selection port 2 - see Table 1-1				
	Data rate selection port 1 - see Table 1-1						
Data rate selection port 1 - see Table 1-1							
							*0 = Operated 1 = Unoperated

## Control Port 2



It is possible to change the V.24 port 1 and 2 configuration whilst the multipoint card is transmitting or receiving data, although a small loss of data may result.

Control Port	1	1	1		1	2	2
Port 1 Rate	D7	D6	D5	Port 2 Rate	D4	D5	D4
19200	0	0	0	19200	0	0	0
9600	0	0	1	9600	0	0	1
4800	0	1	0	4800	0	1	0
2400	0	1	1	2400	0	1	1
1200	1	0	0	1200	1	0	0
600	1	0	1	600	1	0	1
Disabled	1	1	1	Disabled	1	1	1

**Table 1-1 Baud rate settings**

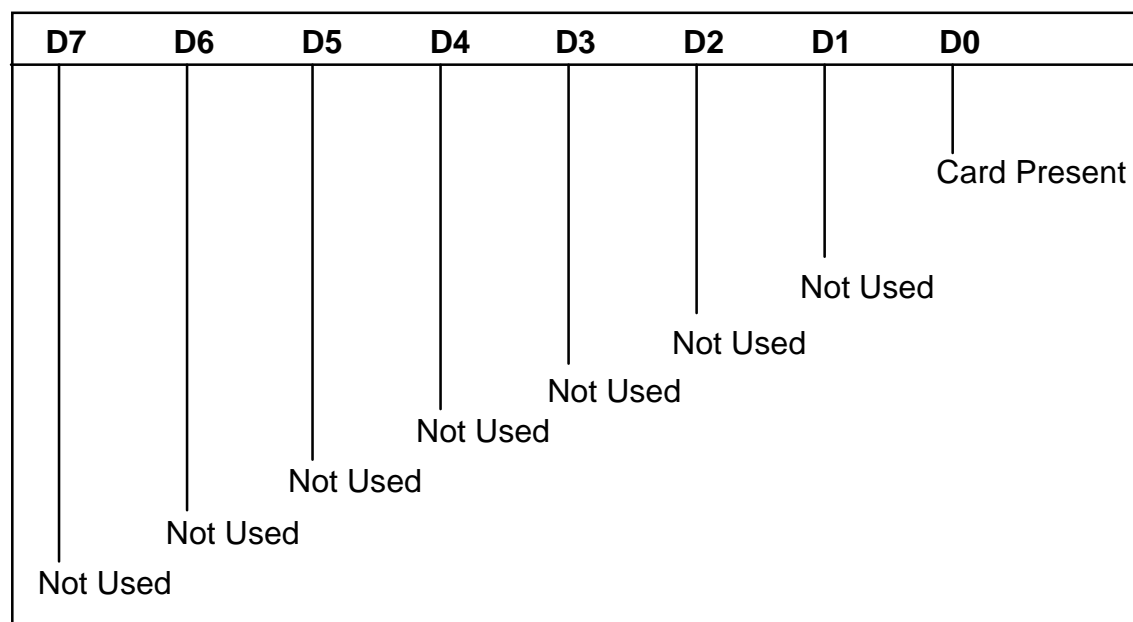
The disable option disables all transmission and reception of asynchronous data for that port, and places FH into the appropriate channel of the 64kbit/s timeslot, allowing two masters to be present in the system, providing they use different ports.

If one channel is set for 19200bps operation, the other channel should be disabled, refer to the basic operation section.

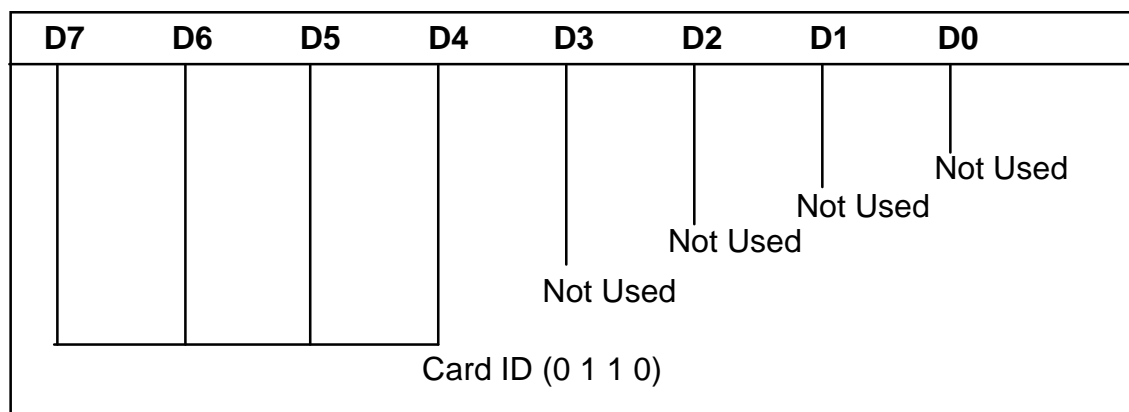
## 7. Status Port Facilities

The status bytes can be monitored from within the multiplexer control software.

Note all signals are active low. 0 = Operated



## Status Port 2



## 8. Links

TL1 and LK2 are used for test purposes only and should be in the upper and left positions respectively.

LK1 must be in the upper position.

## 9. Switches

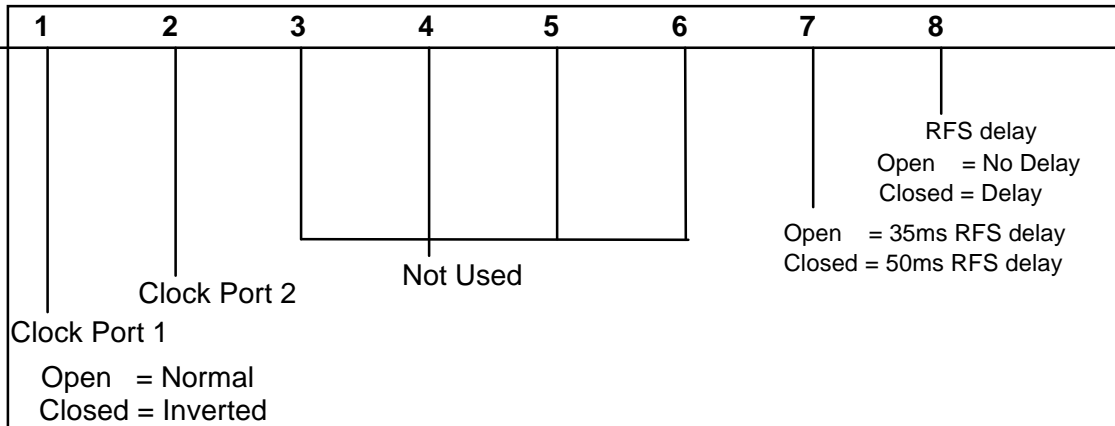
Receive Data (output) is clocked out on the rising edge of the V.28 clock selected, and the Transmit Data (input) is sampled on the falling edge. Under normal operating conditions this ensures that incoming data is sampled in the centre of each bit. If however long propagation delays mean that the incoming data is now changing close to the falling edge of the clock then S1 can be used to select sampling on the rising edge instead.

This switch also controls the delay imposed on RFS (output) being asserted after RTS (input) has been asserted.

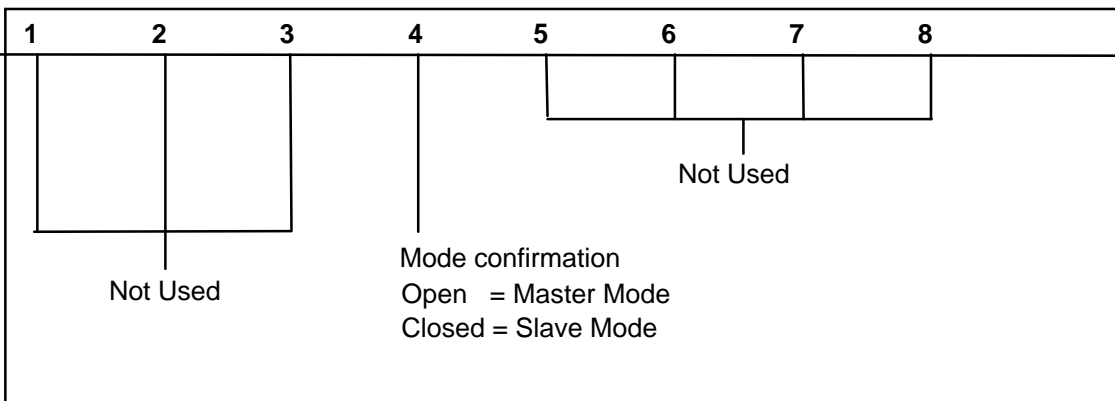
Switch S2-4 must be used in conjunction with the setting of bit D7 of Control Port 2 in order to select Master mode. If either is set to Slave then Slave will be selected.

The switches are defined below:-

### S1



### S2



## 10. Interface connections

Signal	CCITT cct	Port 1	Port 2	V.24 Interface
TD	103	4c(3)	12c(9)	2
RD	104	8c(7)	16c(13)	3
RTS	105	3c(2)	11c(8)	4
RFS (CTS)	106	7c(6)	15c(12)	5
DSR	107	5b(29)	13b(35)	6
DTR	108	4b(28)	12b(34)	20
RLSD	109	5c(4)	13c(10)	8
SG	102	2c(1)	10c -	7

Earth from the multiplexer backplane is on pins 2b, 10b, 18b and 26b  
Numbers in brackets are those on the DT280 50 way Amphenol connector.