

# **Dual Nx64k Data Card Operating Information**

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## STATUTORY NOTICES

### APPROVAL

The Case Technology Dual Nx64k interface card is approved for connection to UK leased line X.21 services when installed in a Case Technology 2000 or 3000 series multiplexer chassis. Any other usage will invalidate any approval given if as a result it ceases to comply with the edition of BS6301 to which it was approved.

The approval number is NS/3660/I/N/603189.

- 1) WARNING. Inter-connection directly, or by way of other apparatus, of ports marked:-  
"SAFETY WARNING. See instructions for use."  
with ports not so marked may produce hazardous conditions on the network. Advice should be obtained from a competent engineer before such a connection is made.
- 2) The safety warning applies to the X.21 interface ports if they are connected to any apparatus other than an NTP. These port do not provide sufficient isolation to satisfy the requirements of BS6301. Apparatus connected to these ports should either have been approved to BS6301 or have previously been evaluated against British Telecom plc (Post Office) Technical Guides 2 or 26 and given permission to attach. Other usage will invalidate any approval given to this equipment.
- 3) The apparatus is not intended to be operated under controlled conditions of ambient temperature and humidity.
- 4) For connection to an NTU, cable assembly type 1520-XXX, available from Case Technology should be used.
- 5) The safety status of the interface is SELV.



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

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All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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# Dual Nx64k Data Card

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## 1. General Description

The DT585 Dual Nx64k interface card provides two independent X.21 Nx64k interfaces suitable for connection to leased line data services or Data Terminal Equipment.

The card can operate in two different modes. 1) Aggregate mode and 2) Channel mode. Each line may be set to carry aggregate data (Aggregate mode) or channel data (Channel mode). The value of N for each line can be individually set to be between 1 and 32 (64 to 2048 kbps) depending upon the multiplexer and position into which it is fitted. Channel Associated Signalling (CAS), A/B Switching and a Management Channel for each line is supported in aggregate mode.

## 2. Operation

The card provides two Nx64k data circuits with V.11 interface levels designated Line 1 and Line 2, each operating independently either as a channel data interface circuit, or as an aggregate. A single card can be configured for a) Both circuits in Aggregate mode, b) Both circuits in Channel mode or c) One in Channel and one in Aggregate mode. There are some bandwidth restrictions when used with early multiplexer firmware releases and these are listed in Section 18. Each circuit may operate without the necessity to provide a control input signal.

Operating in Aggregate or Channel mode, the card provides one or two X21, Nx64k circuits with a combined maximum rate of data of 1984kbps when fitted in 2000 series multiplexers, or 2048kbps in a 3000 series multiplexer in ports 3 or 4. When fitted in ports 1 or 2 of a 3000 series multiplexer *each* circuit may operate at up to 2048kbps.

In either mode of operation the card can provide derived clocks at 8kHz or 2048kHz for synchronisation of the multiplexer, however only the 8kHz clock can be used in a 2000 series multiplexer. The card can function in Modem, DCE or DTE mode. Test loops are provided on a per circuit basis.

### 3. Specifications

Data Rate:-	64kbps to 2048kbps.
Interface:-	Conforms to CCITT X.21 with V.11 electrical levels.
Byte Timing:-	Conforms to CCITT X.24.
Control Signals:-	Leased Line X.21 Control Signals, 'C' and 'I' (Control and Indicate) are supported for each line.
Delay:-	The delay from the X.21 interface to the multiplexer backplane is typically 250us for each direction of transmission. Maximum 1ms.
Quantisation distortion:	The quantisation distortion through the card for a digitally encoded VF circuit is zero.
Power consumption:-	10 Watts maximum. <b>Caution:-</b> A maximum of 8 DT585 cards may be fitted to the channel card positions in any one multiplexer chassis.

### 4. Timeslot Allocation

#### 4.1 General

There are 32 timeslots (2048k), on the backplane ports of a 3000 series multiplexer, which are numbered TS0 to TS31 and these may all be used for allocation to a circuit. Note that TS0 does not contain any G704 framing and is simply another 64k data circuit to the backplane ports. There is no access to TS0 in 2000 series multiplexers which have TS1 to TS31 (1984k) only available.

Timeslot requirements are different for each mode of operation, physical position and the type of multiplexer into which it is installed.

## **4.2 Channel Mode**

- a) 2000 series and 3000 series ports 3 and 4

Timeslots may be allocated to either circuit on the card without restriction and do not have to be consecutive. The resulting speed of the channel interface circuit is determined by the N value set on the control port. An equivalent number of timeslots must also be allocated to the circuit.

- b) 3000 series ports 1 and 2

Timeslots are automatically allocated consecutively to each line starting at TS0 by setting the N value for the line. Each line will interface directly to the appropriate stream depending on its fitted position and the selected line, e.g. Port 1 Line 1 will interface to S1 and Port 2 Line 2 to S4 on the cross-connect switch.

## **4.3 Aggregate Mode**

- a) 2000 series and 3000 series ports 3 and 4

Timeslots may be allocated to each circuit without restriction. The first timeslot i.e. lowest numbered timeslot allocated, will be used for framing, management and signalling and can therefore not be used as a 64k channel in the Nx64k interface circuit.

- b) 3000 series ports 1 and 2

When installed in ports 1 and 2 of a 3000 series multiplexer Line 1 will automatically interface to S1 (S3) and Line 2 to S2 (S4) respectively. It is only necessary to set the N value of the line, such that if, for example, the N value is set to 4 for the line, it will interface to timeslots 0 to 3 at the stream port; and if set to 12 it will interface to timeslots 0 to 11. Note that the timeslots are consecutive but may be cross connected without restriction using the 3000 multiplexer cross-connect facilities. TS0 will always be used to carry the frame synchronisation, etc.

- c) Framing

Framing for the Nx64k line is generated on the card. Bits 1 and 2 of the first timeslot allocated to the line are used for frame synchronisation and management and the card will overwrite any data in these bits that are allocated to the card. If a timeslot carrying a 48k data channel is cross connected to the first allocated timeslot, the data will be placed in bits 3 to 8 with any control signal carried in bit 1 being lost.

## 6. 48kbps Data Channel

In aggregate mode, without CAS, bits 3 to 8 of the first timeslot allocated are available for use as a 48kbps data channel. This channel may be allocated to a channel interface card operating at 48kbps in the normal way.

## 5. Signalling

In aggregate mode, Channel Associated Signalling (CAS) may be used and this is carried in the first allocated timeslot. Two bits of the 48k available are used for the multiframe synchronisation pattern and the remaining four for the signalling information. The multiframe length may be selected to be either 16 or 32 frames. If a 16 multiframe is selected only the first 16 x 64k channels may have CAS with a maximum signalling distortion of 2ms. If a 32 multiframe is selected all 64k circuits may have CAS but the maximum signalling distortion will increase to 4ms.

## 7. Management

Management channels are only available when operating in aggregate mode in 3000 series multiplexers. The 4kHz sampled management channels from the two circuits are pre-assigned, as bi-directional transmission paths with Line 1 connected to M1 and Line 2 connected to M3. The management is multiplexed on to the Nx64k line with one I/P and one O/P available at the V.28 I/O connector. Direct routing of management to the system controller is possible. The management routing is shown in Appendix A. Note that it is necessary to change the EPLD for uni-directional working, contact Cray Communications for details. The channel may be used to carry 1200bps async management data.

**Note:** DT585 Build Level 1 Hardware has some limitations, which make it suitable only for point to point management links. The main limitations are:

- i) Application of loops may cause the management system to fail due to the NCS receiving its own polling.

- ii) There are no programmable patchfield facilities, although patchfields may be tailored to customer needs. Contact Cray Communications for details.
- iii) There is no cross-connection of management bits between the two lines. As a consequence the standard patchfield does not support a delta network.

## **8. Synchronisation**

### **8.1 Multiplexer Synchronisation**

Each line has independent synchronisation circuits enabling each one to run at different values of N. Clock signals at 2048kHz and 8kHz are derived independently from both Line 1 and Line 2 Terminal Timing (TT) inputs for DTE mode, and these may be used to synchronise the multiplexer. The 2048kHz clocks may be used in the 3000 series multiplexer automatic clock monitoring scheme; and the 8kHz clocks may be used in any multiplexer where Line 1 will provide 8k1 and Line 2 will provide 8k2. The 8kHz clocks may be isolated from the system by link selection.

### **8.2 Nx64k Interface Synchronisation**

Each Nx64k interface transmit (output) and receive (input) data buffer clocks, may be independently selected by the Control Port to be driven from one of the following sources:-

- a) Multiplexer (System) clock at Line 1 rate. Nx64k value
- b) Multiplexer (System) clock at Line 2 rate. Nx64k value
- c) Line 1 Terminal Timing input
- d) Line 2 Terminal Timing input

These synchronisation options will allow independent Modem, DCE or DTE operation for the two lines. The interface and system clocks must be frequency locked; buffering is provided to allow for phase and jitter.

Byte Timing is provided in channel mode for each line and this may be enabled or disabled by software selection. Note that Byte Timing or an 'Indicate' output is available by link selection (See 10.2).

## **9. A/B Switching**

In order to provide resilience for a single aggregate link failure, the two Nx64k interfaces can be configured for A/B switching. Two separate network connections are then made with automatic switching between the two routes. For this option to function both lines must be configured exactly the same and be operating in aggregate mode.

If A/B switching is enabled, data from the multiplexer backplane will be simultaneously broadcast to both line outputs. Incoming data will be routed to a common backplane port and sourced from either Line 1 or Line 2 depending upon the current fault conditions on the line. When fitted to P1 or P2, the common backplane port is S1 (S3). When fitted to P3, P4 or a 2000 series multiplexer, the common backplane port is all timeslots assigned to circuit (Line) 1. If the working line fails due to loss of frame sync it will automatically switch to the other line if that is in a fault free condition, otherwise it will not switch. If both have failed the first one to recover will be selected.

## **10. Configuration**

The DT585 is configured by a combination of Control Ports, Links and Switches. Cards that are installed in a multiplexer chassis fitted with DT981/6 or later firmware on the system control card can be configured using a menu structure obviating the necessity to set the control ports. This facility is described in section 10.3.

### **10.1 Control Ports**

The following parameters are set using the control ports:-

- a) D0 Line 1 loop/slip LED
- b) Clock selection for the input and output data buffers
- c) Aggregate or Channel mode of operation
- d) Data Loops
- e) CAS mode
- f) Length of the CAS Multiframe
- g) A/B Switching Mode
- h) Byte Timing

The control port bits are set and displayed in the following order in the multiplexer configuration menu and should be set to a 1 or a 0 as required.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

**a) Circuit 1 Control Port 1**

D7	A0	Line 1 I/P clock selection
D6	A1	" " " "
D5	A0	Line 1 O/P clock selection
D4	A1	" " " "
D3		A/B mode. 0=enabled 1=disabled
D2		Line 1 Multiframe Length. 0=16 frames 1=32 frames
D1		Line 1 Loop. 0=looped 1=not looped
D0		Line 1 Loop/Slip LED. 0=lit 1=not lit

Note that D0 and D1 are for maintenance purposes and should be set to 1.

**Clock Selection Bits**

A0	A1	
0	0	System clock at Line 1 Nx64k value
0	1	System clock at Line 2 Nx64k value
1	0	Sourced from Line 2 TT input
1	1	Sourced from Line 1 TT input

**b) Circuit 1 Control Port 2**

D7	Line 1 Operating Mode 0=Channel mode 1= Aggregate mode
D6	Line 1 CAS or Byte Timing 0=disabled 1=enabled
D5 to D0	Line 1 'N' rate. Set to equivalent Binary value required

Note that CAS only operates in Aggregate mode and Byte Timing in Channel mode

### c) Circuit 2 Control Port 1

D7	A0	Line 2 I/P clock selection
D6	A1	" " " "
D5	A0	Line 2 O/P clock selection
D4	A1	" " " "
D3		Not used , set to 1
D2		Line 2 Multiframe Length. 0=16 frames 1=32 frames
D1		Line 2 Loop. 0=looped 1=not looped
D0		Line 2 Loop/Slip LED. 0=lit 1=not lit

Note that D0 and D1 are for maintenance purposes and should be set to 1

### Clock Selection Bits

A0	A1	
0	0	System clock at Line 1 Nx64k value
0	1	System clock at Line 2 Nx64k value
1	0	Sourced from Line 1 TT input
1	1	Sourced from Line 2 TT input

### d) Circuit 2 Control Port 2

D7	Line 2 Operating Mode	0=Channel mode 1=Aggregate mode
D6	Line 2 CAS or Byte Timing	0=disabled 1=enabled
D5 to D0	Line 2 'N' rate.	Set to equivalent Binary value required.

Note that CAS only operates in Aggregate mode and Byte Timing in Channel mode.

## 10.2 Links and Switches

### a) Links

LK1 to LK4 Test links. These must be fitted in position 2-3  
LK5 and LK6 selects the control output at the interface to be either the X.21 (I) Indicate lead or the X.21 (B) Byte Timing output.

LK5	Line 2	1-2=Control Indicate.	2-3=Byte timing
LK6	Line 1	1-2=Control Indicate.	2-3=Byte timing

The control Output will be set to 'On' after initial power up in accordance with the requirements of NET1.

LK7	M1 Management select. See section 19
LK8 & LK15	M3 Management select. See section 19
LK9	8k2 clock select. 1-2=disconnected. 2-3=connected
LK10	8k1 clock select. 1-2=disconnected. 2-3=connected
LK11	Line 2 Data Invert. 1-2=Normal. 2-3=Inverted
LK12	Line 1 Data Invert. 1-2=Normal. 2-3=Inverted
LK13	Line 2 Clock Inversion. 1-2=Normal. 2-3=Inverted
LK14	Line 1 Clock Inversion. 1-2=Normal. 2-3=Inverted
LK13 and LK14	are intended for use when the card is used as a DCE and the round trip data delays, particularly at high N values, require inversion of the clock in order to prevent mis-clocking of input data by the card.

## b) Switches

There is one 8 pole DIL switch on the card designated S1 which is used to set a special frame synchronisation pattern used during initialisation and re-synchronisation of the Nx64k link in aggregate mode. The switch setting applies to both lines and the setting **MUST** be the same at both ends of the link. Switches 1 and 2 are not used, the remaining six, 3-8, may be set in any combination of Open and Closed except that all 'Open' is an invalid setting and will result in the lines failing to synchronise.

## 10.3 Configuration by Menu Options

Dual Nx64k cards installed in a 3000 series chassis fitted with DT981/6 or later firmware have menu options incorporated to simplify configuration of the card. The links and switches will still have to be set but the following menu options are available to replace the Control Port settings if desired.

The menus present a sub set of possible configurations for the card which when used will modify the control port settings as necessary.

Access to the menu options, which will only be displayed for a slot fitted with an Nx64k card, is by selecting 'Port' from the 'Modify' sub menu whereupon the operator will be prompted for the port number and in the case of ports 3 and 4 for the card slot.

The following menu structure will be displayed:-

```
(CCEM) Port | sYnc | Alarms | Cross connect >P
(CCEMP) Assigned cct | Circuit ctl | Smart configs | p1 | p2 | p3 | p4 >3
(CCEMP3) A | B | C | D | E | F | G >A
(CCEMP3A) Mode | Clock mode | N rate >
```

### 10.3.1 Mode menu

```
(CCEMP3A) Mode | Clock mode | N rate >M  
1 Aggregate (Framed)  
2 Channel (Unframed)  
Mode 1 >1
```

If aggregate (framed) mode is selected, then the following prompts for A/B mode and signalling options are displayed:

```
1 A/B enabled  
2 A/B disabled  
Mode 1 >2  
1 CAS First 16 channels  
2 CAS All channels  
3 Non CAS  
Mode 1 >3
```

If Channel mode (unframed) mode is selected the following prompt will be displayed:

```
1 Byte timing enabled  
2 Byte timing disabled  
Mode 1 >2
```

### 10.3.2 Clock mode menu

This command allows the user to make the clock mode selection for the input and output lines 1 and 2, or both lines simultaneously when in A/B switching mode. The prompts for Line 1 and Line 2 will not be displayed in A/B switching mode since both lines must be the same.

```
(CCEMP3A) Mode | Clock mode | N rate >C  
(CCEMP3AC) line 1 | line 2 >1  
1 DCE  
2 DTE  
3 Modem  
mode 1 >2
```

### 10.3.3 N Rate menu

This command allows the user to set up the data rate for each line in multiples of 64k. In A/B switching mode, the option to set Line 1 or Line 2 will not be displayed since both lines must be configured to run at the same speed.

(CCEMP3A) Mode | Clock mode | N rate >N

(CCEMP3AN) line 1 | line 2 >1

1 =	64	2 =	128	3 =	192	4 =	256
5 =	320	6 =	384	7 =	448	8 =	512
9 =	576	10 =	640	11 =	784	12 =	768
13 =	832	14 =	896	15 =	960	16 =	1024
17 =	1088	18 =	1152	19 =	1216	20 =	1280
21 =	1344	22 =	1408	23 =	1472	24 =	1536
25 =	1600	26 =	1664	27 =	1728	28 =	1792
29 =	1856	30 =	1920	31 =	1984	32 =	2048

Bit rate = Undefined >12

Undefined indicates that an invalid setting has been selected e.g.50, or that the system cannot decode the control port setting. Once a valid rate has been set the display will show the current rate for the line:

Bit rate = 12\*64kb/s (768kb/s)

### 10.3.4 Display Format

The settings for both Line 1 and Line 2 will be displayed from a single menu selection:

(CCED) Load | Save | Modify | Display >D

(CCED) Port | sYnc | Alarms | Cross connect >P

(CCEDP) Assigned cct | Circuit ctl | Smart configs | p1 | p2 | p3 | p4 >3

(CCEDP3) A | B | C | D | E | F | G >A

Dual N \* 64 Card fitted

A/B Mode disabled

Line 1

Aggregate (Framed), CAS First 16 channels

Clock mode = DTE

BitN rate = 12\*64kb/s (768kb/s)

Line 2  
Channel (Unframed), Byte timing disabled  
Clock mode = Modem  
BitN rate = 20\*64kb/s (1280kb/s)

Or alternatively if A/B mode is enabled:

(CCEDP) Assigned cct | Circuit ctl | Smart configs | p1 | p2 | p3 | p4 >3  
(CCEDP3) A | B | C | D | E | F | G >A

Dual N \* 64 Card fitted  
A/B Mode enabled

Line 1/2  
Aggregate (Framed), CAS first 16 channels  
Clock mode DCE  
BitN rate = 4\*64kb/s (256kb/s)

## 11. Control Signals

The card provides X.21 conformant leased line control signals, 'C' and 'T' for each line. If the control input is in the OFF state all V.11 data input to the card will be set to 1's thus preventing the transmission of data; in aggregate mode this will cause loss of input synchronisation. The control input open circuit condition is 'ON' which will allow the data circuit to operate. The control O/P is set to 'ON' except at power up when it pulses 'OFF' for one second. The control signals are not passed across the link.

In Loop, the control input (C) is connected directly to the control output (I) of the interface.

## 12. LED Indicators

Four LED indicators are provided on the card displaying the following when lit:-

Top	RED	Line 2 Alarm 2 fault or looped
	GREEN	Line 2 Aggregate mode
	RED	Line 1 Alarm 2 fault or looped
	GREEN	Line 1 Aggregate mode

## 13. Test Loops

Independent test loops are provided for each line in accordance with CCITT X.150 3c at the V.11 interface, looping both data and control signals. The loop is applied just after the V.11 drivers and receivers and loops towards the multiplexer backplane.

*CAUTION A loop may cause management signals to be looped back to themselves resulting in loss of control.*

## 14. Alarms

### 14.1 Alarm Responses

The card detects the following faults on a per circuit basis which are displayed in Status Port 1 for each circuit.

FAULT	SLIP	ALARM 2	STATUS PORT1 BIT
Input buffer slip	Yes	No	D2=0
Loss of receiver frame sync	No	Yes	D5=0
Loss of Multiframe sync	No	Yes	D6=0
In channel mode only slip is detected			

### 14.2 Slip Detection

The card provides Slip detection for each of the Nx64k input data buffers. The data buffer depth is 8 frames. During a controlled slip both the input and output buffers are reset.

If necessary, for special applications, the depth of the buffer may be altered by changing an EPLD. Contact Cray Communications for details if this is required.

## 15. Status Ports

The Status Ports indicate the status of the card and can be displayed in the 'Maintenance' menu of the multiplexer. The bits are displayed in the same manner as the control port bits (see section 9.1), and in the case of alarms, a zero (0), will indicate a fault condition. The normal bit values for card identity and other information are shown in brackets.

### **a) Circuit 1 Status Port 1**

D7	Card ID (1)
D6	Line 1 Multi Frame Sync loss
D5	Line 1 Frame Sync loss
D4	Circuit 1 Alarm 2
D3	Spare (1)
D2	Line 1 Slip
D1	Card ID (1)
D0	Circuit 1 present (0)

### **b) Circuit 1 Status Port 2**

D7	Card ID (1)
D6	Card ID (0)
D5	Card ID (0)
D4	Card ID (1)
D3	Spare (1)
D2	Spare (1)
D1	Line 2 Remote Sync Loss
D0	Line 1 Remote Sync Loss

In the alarm condition (0), D0 and D1 indicate that the remote end has failed to synchronise to the incoming synchronisation pattern, they only function in Aggregate mode and will be set to 1 in Channel mode.

### **c) Circuit 2 Status Port 1**

D7	Card ID (1)
D6	Line 2 MF Sync loss
D5	Line 2 Frame Sync loss
D4	Circuit 2 Alarm 2
D3	Spare (1)
D2	Line 2 Slip
D1	Spare (1)
D0	Circuit 2 present (0)

Circuit 2 Status Port 2 is not used and will be set to all 1's.

## 16. I/O Pin Connections

The following pin connections are as viewed on the multiplexer DIN 41612 I/O connector with connections for the Amphenol 50 way female connector in brackets. (A) and (B) are the balanced pair of the V.11 signals.

ROW A		ROW C		TITLE
32a	(50) Line 2 RD (B)	32c	(25) Line 2 RD (A)	Data Output
31a	(49) Line 2 ST (B)	31c	(24) Line 2 ST (A)	Clock Output
30a	(48) Line 2 RT (B)	30c	(23) Line 2 RT (A)	Clock Output
29a	(47) Line 2 I (B)	29c	(22) Line 2 I (A)	Control Output
28a	(46) Line 2 SD (B)	28c	(21) Line 2 SD (A)	Data Input
27a	(45) Line 2 TT (B)	27c	(20) Line 2 TT (A)	Clock Input
26a	Earth	26c	Sig Gnd	
25a		25c		
24a	(44)	24c	(19)	
23a	(43) Line 2 C (B)	23c	(18) Line 2 C (A)	Control Input
22a	(42)	22c	(17)	
21a	(41)	21c	(16)	
20a	(40)	20c	(15)	
19a	(39)	19c	(14)	
18a	Earth	18c	Sig Gnd	
17a		17c		
16a	(38) Line 1 RD (B)	16c	(13) Line 1 RD (A)	Data Output
15a	(37) Line 1 ST (B)	15c	(12) Line 1 ST (A)	Clock Output
14a	(36) Line 1 RT (B)	14c	(11) Line 1 RT (A)	Clock Output
13a	(35) Line 1 I (B)	13c	(10) Line 1 I (A)	Control Output
12a	(34) Line 1 SD (B)	12c	(9) Line 1 SD (A)	Data Input
11a	(33) Line 1 TT (B)	11c	(8) Line 1 TT (A)	Clock Input
10a	Earth	10c	Sig Gnd	
9a		9c		
8a	(32)	8c	(7)	V28 Management Output
7a	(31) Line 1 C (B)	7c	(6) Line 1 C (A)	Control Input
6a	(30)	6c	(5)	
5a	(29)	5c	(4)	V28 Management Input
4a	(28)	4c	(3)	
3a	(27)	3c	(2)	
2a	(26) Earth	2c	(1) Sig Gnd	
1a		1c		

Note that the Control outputs may be either the X.21 Indicate or Byte timing output.

## 17. I/O Adapters DT584, DT582 and DT599

### a) DT584

DIN 41612 to 2 x 15 way male 'D' type connectors (X.21 pin out). Intended for connection to a leased line DCE port. The pin out for each connector is identical, the top 'D' type is connected to Line 2, the lower to Line 1.

<b>'D' pin No.</b>	<b>Name/Function</b>
2	T (A) data o/p
9	T (B) data o/p
3	C (A) control o/p
10	C (B) control o/p
4	R (A) data i/p
11	R (B) data i/p
5	I (A) control i/p
12	I (B) control i/p
6	S (A) clock i/p
13	S (B) clock i/p
8	Signal ground

### b) DT582

DIN41612 to 1 x 15 way 'D' type male connector DTE, top 'D' type, connected to Line 2 and 1 x 15 way 'D' type female connector DCE, lower connected to line 1. This is intended for use in applications where leased line emulation is required, e.g. for connection to LAN bridge, and connection to a leased line is required. This would allow, in principle, the LAN bridge to be interfaced on to a leased line.

#### **DTE upper 'D' type**

<b>'D' pin No.</b>	<b>Name/Function</b>
2	T (A) Data o/p
9	T (B) data o/p
3	C (A) control o/p
10	C (B) control o/p
4	R (A) data i/p
11	R (B) data i/p
5	I (A) control i/p
12	I (B) control i/p
6	S (A) clock i/p
13	S (B) clock i/p
8	Signal ground

## DCE lower 'D' type

<b>'D' pin No.</b>	<b>Name/Function</b>
2	T (A) data i/p
9	T (B) data i/p
3	C (A) control i/p - (see note a)
10	C (B) control i/p " "
4	R (A) data o/p
11	R (B) data o/p
5	I (A) control o/p (see note a)
12	I (B) control o/p " "
6	S (A) clock o/p
13	S (B) clock o/p
7	X or B (A) (see note b)
14	X or B (B) " "
8	Signal ground

### c) DT599 DCE

DIN 41612 to 2 x 15 way 'D' type female connectors providing two DCE interfaces. The pin connections for each line are identical.

<b>'D' pin No.</b>	<b>Name/Function</b>
2	T (A) data i/p
9	T (B) data i/p
3	C (A) control i/p - (see note a)
10	C (B) control i/p " "
4	R (A) data o/p
11	R (B) data o/p
5	I (A) control o/p (see note a)
12	I (B) control o/p " "
6	S (A) clock o/p
13	S (B) clock o/p
7	X or B (A) (see note b)
14	X or B (B) " "
8	Signal ground

**Notes:**

- a) These control inputs and outputs are hard wired together.
- b) These pins may be, via link selection on the I/O adapter, clock input (X) or Byte timing output (B). LK5 and 6 must be set appropriately on the DT585 for Byte timing output.

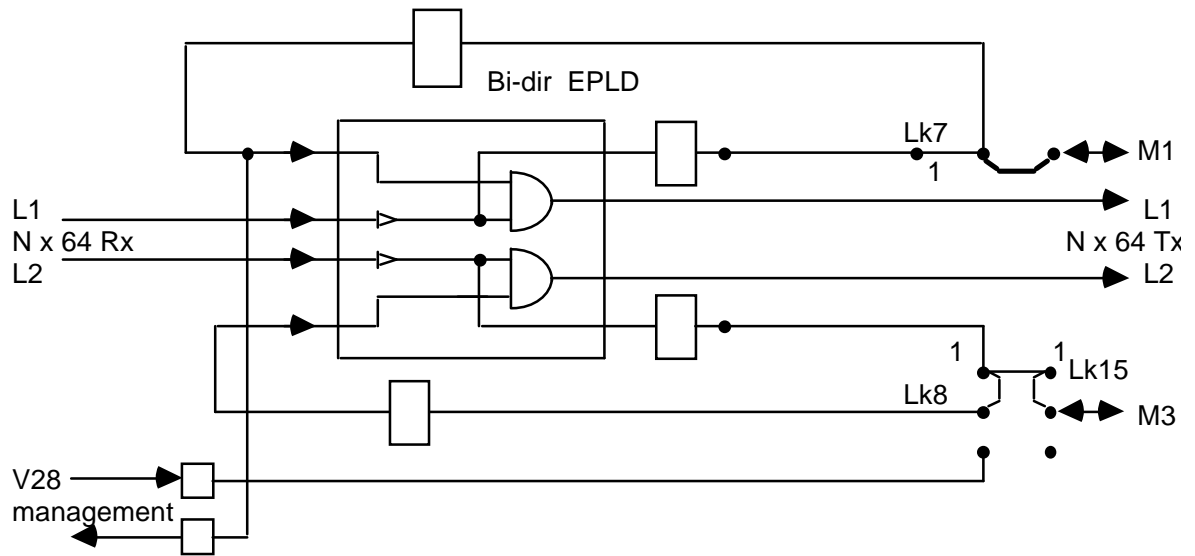
## **18. Firmware Compatibility**

Early versions of the 3000 series operating firmware have limitations affecting the card when fitted into ports 3 or 4. All versions of DT980, DT981/1 and DT981/2 do not have the facility to access TS0 in these ports, The card will function as if it were fitted to a 2000 series multiplexer i.e. with only 31 timeslots available.

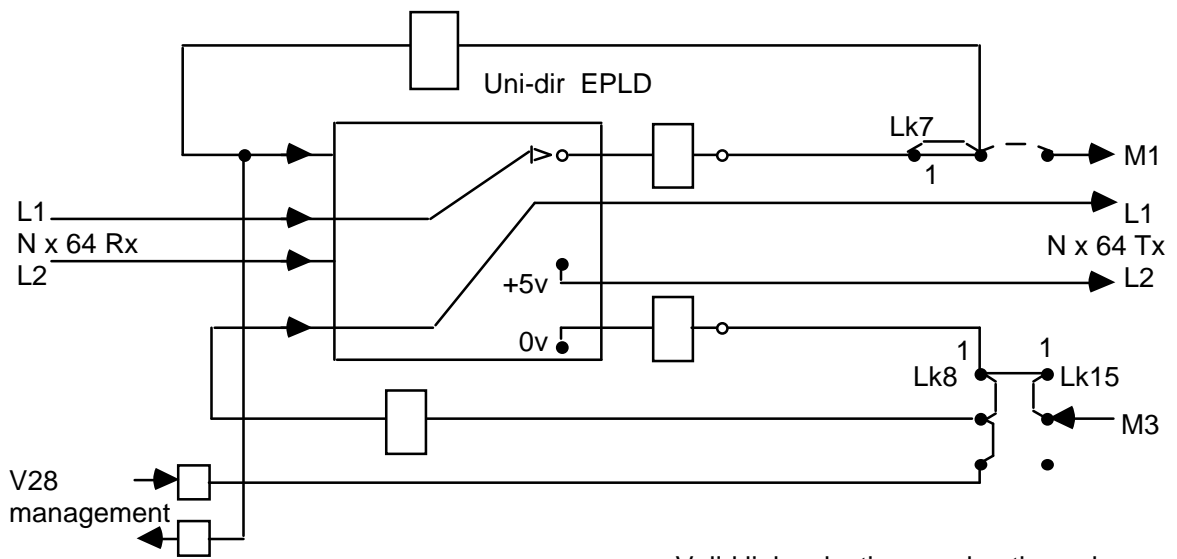
**Note:** DT981/6 Supports user friendly intelligent menus to aid the set-up of the DT585 for common configurations, refer to section 10.3 for more information.

# 19. Management Configuration

## 19.1 Bi-directional Routing



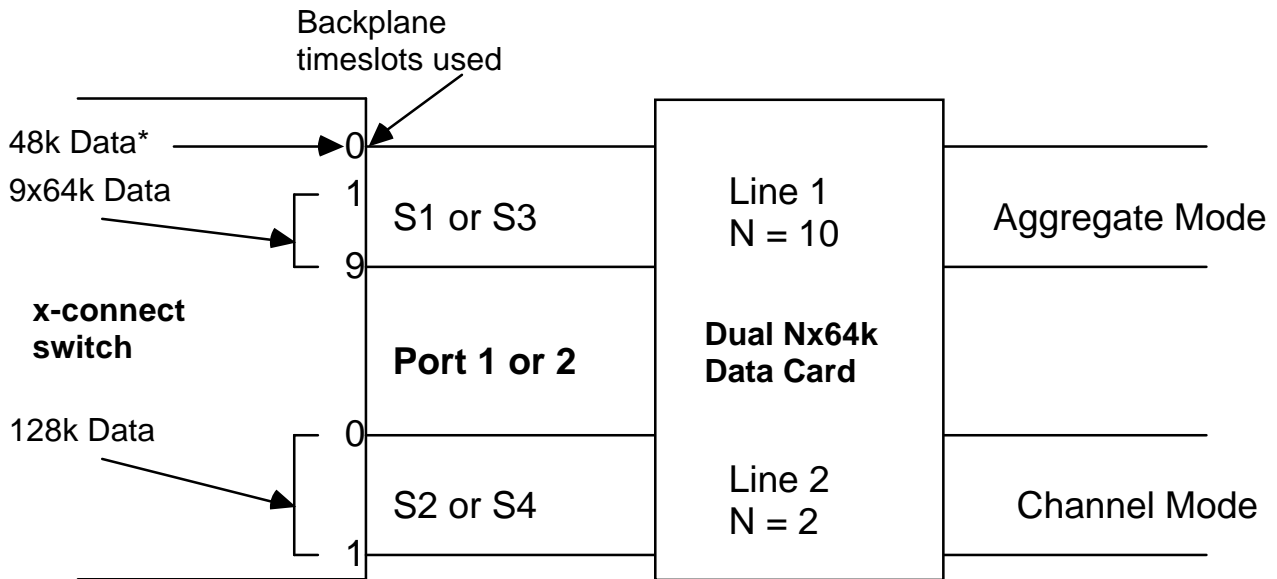
## 19.2 Uni-directional Routing



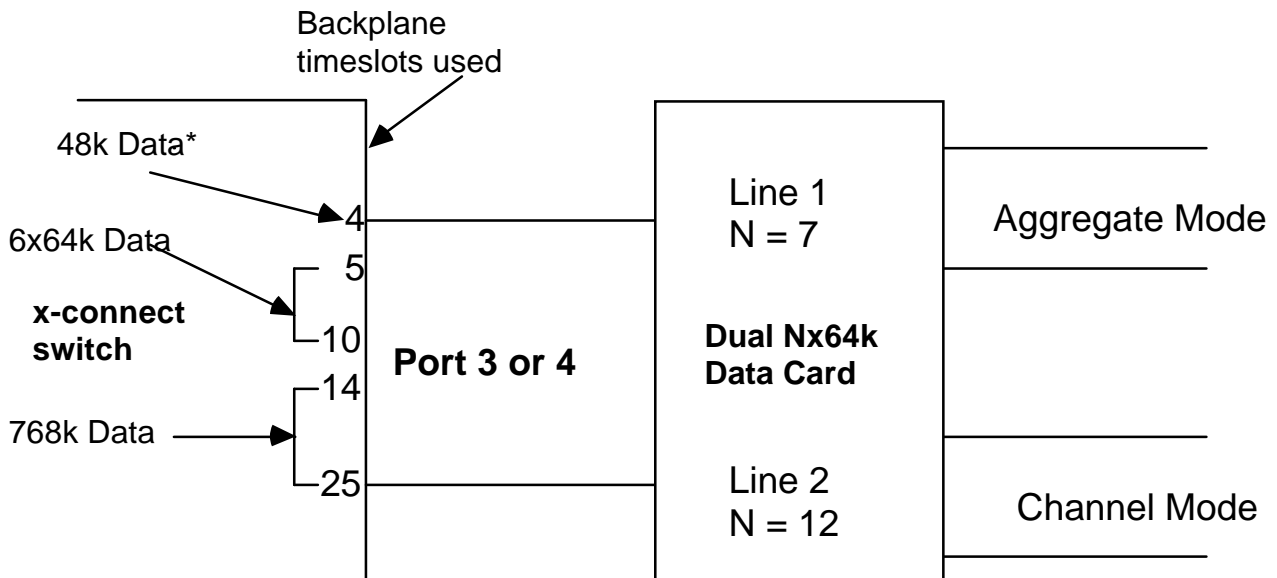
Valid link selections and options shown

## 20. Timeslot Allocation Diagrams

The following diagrams illustrate the allocation of timeslots in a 3000 series multiplexer.

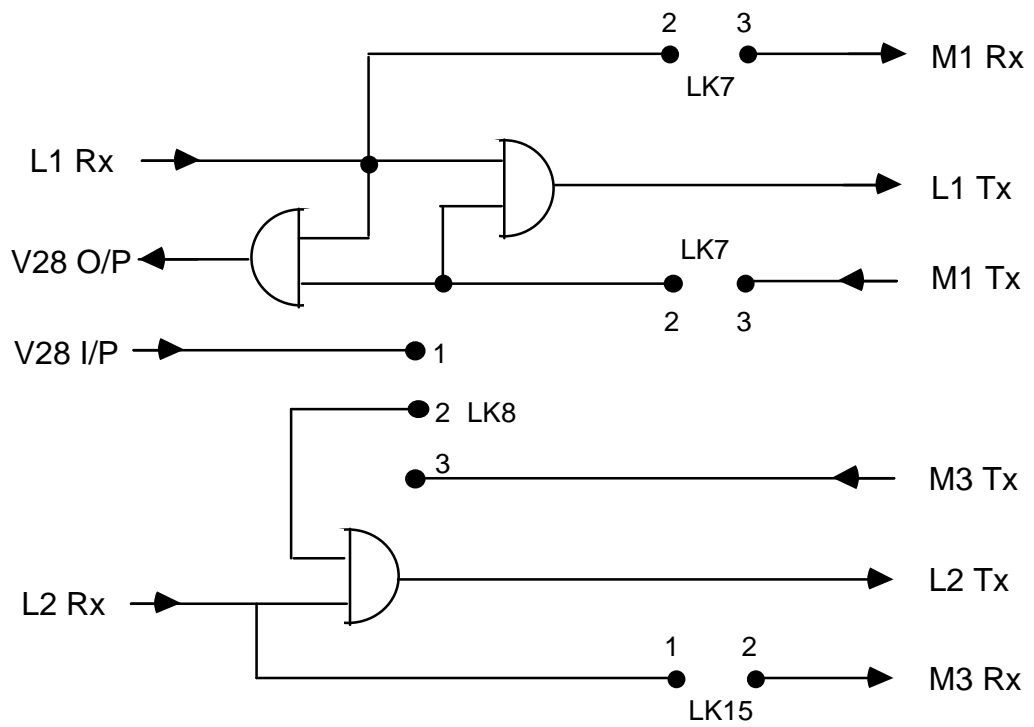


\* 48k Data may be cross-connected if required in to Timeslot 0 if signalling is not used on the aggregate link  
 Backplane timeslots do not have to be allocated



\* 48k Data may be cross-connected if required in to Timeslot 4 if signalling is not used on the aggregate link  
 Timeslots 4-10 for Line 1 are allocated to Circuit 1  
 Timeslots 14-25 for Line 2 are allocated to Circuit 2

## Bi-Directional Management Routing



Note that LK7 is one link which completes both of the connections shown.

## Uni-Directional Management Routing