

E & M Signalling Card Reference Manual

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STATUTORY NOTICES

APPROVALS

The 24 Channel E & M Signalling Card, DTE62, is approved for indirect connection to Telecommunications Systems under the General Approval Number NS/G/1234/J/100003. This card does not contain any isolation barriers, and any apparatus connected to it must conform to the requirements of the General Approval.

The safety status of all ports is SELV.

All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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Published by Case Technology Technical Publications Department

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E & M Signalling Card

1. Description

The DTE62 comprises a DT545 fitted with DT971/1 firmware.

the card provides an electrical interface for 24 E & M signalling channels and can interface to either data or signalling timeslots on the multiplexer backplane. This gives the card two modes of operation, channel associated signalling mode and data mode.

2. Operation

2.1 CAS Mode

In CAS mode, the card will interface to the Drop and Insert signalling busses on the multiplexer backplane. Data timeslots are unaffected. CAS signalling nibbles dropped and inserted to and from these busses will support either 1 or 2 E & M signalling channels as follows:-

a b c d

A B 0 1

A = signalling channel for first E & M Circuit

B = signalling channel for second E & M Circuit, or value set by a link if single channel operation selected.

The selection of 1 or 2 channel operation is via switches, each CAS nibble being independently controlled.

If single channel operation is selected for a nibble, the 'E' interface associated with the 'B' bit is forced to the 'Earth off' condition. The associated 'M' interface is not used, (the outgoing 'B' bit state is set by link LK1, see section 4.2).

The normal signalling function of the 'E' and 'M' wires is as follows:-

Active signalling: closed 'M'-wire results in closed 'E'-wire when the signalling bit is set to logical 0.

Non active signalling: open 'M'-wire results in open 'E'-wire when the signalling bit is set to logical 1.

Up to 12 CAS signalling nibbles may be allocated to the card. The 24 E & M signalling channels are allocated to bits in the CAS nibbles as follows:-

TIMESLOT	A	B	
S	E/M1	E/M2	
S+1	E/M3	E/M4	
S+2	E/M5	E/M6	
S+3	E/M7	E/M8	
S+4	E/M9	E/M10	
S+5	E/M11	E/M12	
S+6	E/M13	E/M14	S = Start timeslot
S+7	E/M15	E/M16	
S+8	E/M17	E/M18	
S+9	E/M19	E/M20	
S+10	E/M21	E/M22	
S+11	E/M23	E/M24	

Note: When used in this mode the card is not allocated timeslots in the normal way, i.e. assigning timeslots to circuits. Instead, timeslots are allocated using control port 1 and control port 2 to specify the start and end timeslots. Timeslots allocated will be sequential from start to end. Timeslots may be allocated which cross TS0, e.g. Start TS28, End TS8, this will allocate 12 timeslots to the card with TS0 being automatically ignored.

All a, b, c and d bits (i.e. signalling, idle code etc.) can be subjected to inversion as specified in section 4.

In normal operation the insert signalling will be disabled during unused timeslots and 1111 is inserted. A selectable option on control port 2 enables the card to insert the idle code '0101' into all unused signalling nibbles.

2.2 Data Mode

In DATA mode, the card will interface to 64kbit/s timeslots on the multiplexer backplane. TS16 signalling nibbles are unaffected. The card may be allocated up to 3 consecutive data timeslots. Each bit of data in these timeslots will be associated with one E & M signalling channel. Thus 24 individual E & M signalling channels are available.

The allocation of E & M signalling channels to the bits in the allocated timeslots will be as follows:-

First Timeslot

BIT1	E/M1
BIT2	E/M2
BIT3	E/M3
BIT4	E/M4
BIT5	E/M5
BIT6	E/M6
BIT7	E/M7
BIT8	E/M8

Second Timeslot

BIT1	E/M9
BIT2	E/M10
BIT3	E/M11
BIT4	E/M12
BIT5	E/M13
BIT6	E/M14
BIT7	E/M15
BIT8	E/M16

Third Timeslot

BIT1	E/M17
BIT2	E/M18
BIT3	E/M29
BIT4	E/M20
BIT5	E/M21
BIT6	E/M22
BIT7	E/M23
BIT8	E/M24

A data bit equal to '1' will present 'earth off' on the 'E' or 'M' interface and data bit equal to '0' will represent 'Earth on'.

Each bit is updated at least every 2ms.

Timeslots are assigned to circuit 1 of the card in the normal way, i.e. not via the control ports.

3. Specifications

3.1 Interface levels:

The 'M' interface meets the following:-

The closed conductor is defined as a closure of the 'M' wire to signalling ground, through a resistance of <1kohm, in series with a voltage in the range -3V to +3V. The current through the resistance is in the range of 5 to 30ma.

The open conductor is defined as the 'M' wire isolated from signalling ground, with the following two test conditions:

- * The open 'M' wire connected to signalling ground, through a resistance of <1kohm, in series with a voltage in the range -20V to -60V.
- * The 'M' wire connected to signalling ground, through a resistance of <10kohm, in series with a voltage in the range -3V to +3V.

The 'M' wire input voltage range is -60V to +3V.

The 'E' interface meets with the following:-

A closed conductor (Earth on) is defined as a closure to signalling ground. The voltage on the 'E' wire is in the range of -1V to +1V, at a current in the external circuit of 5 to 50ma.

An open conductor (Earth off) is defined as a closure to signalling ground. The leakage current is <40µa.

The 'E' wire is protected against over voltage in the power range <1 Watt.

Signalling Distortion: The signalling distortion per 500bit/s signalling channel is less than 3ms (excluding noise filter).

Signalling Ground: The 'E' wire is connected to equipment ground, or external ground via link selection.

3.2 Performance

TS16 E & M signalling bits

Bits 'a' and 'b' in TS16, according to CCITT rec.G.704 table 7, are used for signalling. Bit 'b' logic levels can be set, via a link, when not used. Bit 'c' is normally fixed to 0 and bit 'd' is normally fixed to 1.

The logic levels of bits a, b, c, d may be individually set (ref. section 4).

Power Requirements: 17 watts (max.) full operation* per card.

* Full operation: All E & M interfaces closed conductor.

4. Link and Switch Settings

4.1 Switch Settings

Switch Open

No inversion of sig. bit 'a'	SW1.8
No inversion of sig. bit 'b'	SW1.7
No inversion of sig. bit 'c'	SW1.6
No inversion of sig. bit 'd'	SW1.5
1 chan. operation for TS S+11	SW1.4
1 chan. operation for TS S+10	SW1.3
1 chan. operation for TS S+9	SW1.2
1 chan. operation for TS S+8	SW1.1
1 chan. operation for TS S+7	SW2.8
1 chan. operation for TS S+6	SW2.7
1 chan. operation for TS S+5	SW2.6
1 chan. operation for TS S+4	SW2.5
1 chan. operation for TS S+3	SW2.4
1 chan. operation for TS S+2	SW2.3
1 chan. operation for TS S+1	SW2.2
1 chan. operation for TS S	SW2.1

Switch Closed

Inversion of sig. bit 'a'
Inversion of sig. bit 'b'
Inversion of sig. bit 'c'
Inversion of sig. bit 'd'
2 chan. operation for TS S+11
2 chan. operation for TS S+10
2 chan. operation for TS S+9
2 chan. operation for TS S+8
2 chan. operation for TS S+7
2 chan. operation for TS S+6
2 chan. operation for TS S+5
2 chan. operation for TS S+4
2 chan. operation for TS S+3
2 chan. operation for TS S+2
2 chan. operation for TS S+1
2 chan. operation for TS S

Where S = start timeslot.

Note: No inversion of signalling bits gives logic levels as per section 2.1 normal signalling.

7. Control Ports

The control ports provide the following facilities:-

7.1 CAS Mode

Control Port 1

D0	Not used
D1	Not used
D2	Not used
D3	Lsb)
D4)
D5) Start timeslot
D6)
D7	Msb)

Control Port 2

D0	Lsb)
D1)
D2) End timeslot
D3)
D4	Msb)
D5	Not used
D6	0 = CAS Mode
D7	0 = no data is inserted into unused CAS nibbles (Drivers open circuit). 1 = 'idle' code inserted into unused CAS nibbles.

For example:

Control Port 1 = 0FH, Control Port 2 = ACH corresponds to the mode of 12 timeslots assigned with the idle code being inserted into unused CAS nibbles.

NOTE: Care must be taken to ensure that the control port settings do not allocate signalling timeslots in use by other cards, as invalid signalling will result.

7.2 Data Mode

Control Port 1

D0 - D7 - Not used

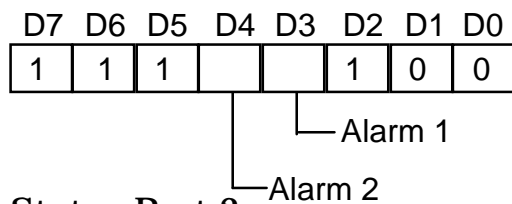
Control Port 2

D0 Not used
D1 Not used
D2 Not used
D3 Not used
D4 Not used
D5 Not used
D6 1 = Data Mode
D7 Not used

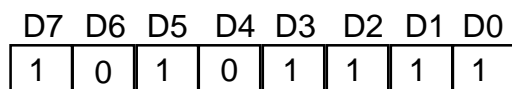
8. Status Ports

The status ports are used to show the current running condition of the circuit, and to display the card identity:-

Status Port 1



Status Port 2



Note: Alarms 1 and 2 are active when low (0).

9. I/O Connections

The connections on the I/O connector for the E & M interfaces are as follows. The pin numbers in brackets are the connections on the 50 Way Amphenol female connector used on the DT280 I/O adapter.

96 way	Signal	96 way	Signal
DIN41612		DIN41612	
		1c	EC
3a (27)	E1	3c (2)	M1
4a (28)	E2	4c (3)	M2
5a (29)	E3	5c (4)	M3
6a (30)	E4	6c (5)	M4
7a (31)	E5	7c (6)	M5
8a (32)	E6	8c (7)	M6
11a (33)	E7	11c (8)	M7
12a (34)	E8	12c (9)	M8
13a (35)	E9	13c (10)	M9
14a (36)	E10	14c (11)	M10
15a (37)	E11	15c (12)	M11
16a (38)	E12	16c (13)	M12
19a (39)	E13	19c (14)	M13
20a (40)	E14	20c (15)	M14
21a (41)	E15	21c (16)	M15
22a (42)	E16	22c (17)	M16
23a (43)	E17	23c (18)	M17
24a (44)	E18	24c (19)	M18
27a (45)	E19	27c (20)	M19
28a (46)	E20	28c (21)	M20
29a (47)	E21	29c (22)	M21
30a (48)	E22	30c (23)	M22
31a (49)	E23	31c (24)	M23
32a (50)	E24	32c (25)	M24

