

Nx64k Card Operating Information

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STATUTORY NOTICES

APPROVALS

The Nx64k Data Card DT530 is approved for indirect connection to Telecommunications Systems under the General Approval Number NS/G/1234/J/100003. This card does not contain any isolation barriers, and any apparatus connected to it must conform to the requirements of the General Approval.

The safety status of the interface is SELV.



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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Nx64k Data Card

1. Description

The Nx64k Data Card DT530 operates as a Data Circuit Terminating Equipment (DCE) to interface between one wide band Data Terminal Equipment (DTE) and channel timeslots in a 30/31 channel 2048kbit/s PCM stream. In this mode send and receive data is clocked in and out using the RT and ST clocks generated on the card.

The card can be used with a limited transmit timing function, i.e. limited DTE operation by DIL switch selection. In this mode send and receive data is clocked in and out using the Terminal Timing input to the card. The card will *not* function as a full DTE.

The unit's data and timing outputs conform to EIA Recommendation RS449 using CCITT V.11 levels, additionally V.35 levels can be used via DIL switch selection. The card will not function with an N value of one.

The DT531 operates exactly as per DT530, except that it can also support transfer of control signals ('C' to 'I') across the PCM stream via Channel Associated Signalling (CAS) stream.

The DT531 can operate in two modes: data only or data plus signalling.

In data only mode, the 'I' output is set permanently on. In data plus signalling mode, the 'C' control input is converted into CAS code as follows and inserted into TS16 CAS channel.

'C'	CAS Code			
	A	B	C	D bit
OFF	1	1	0	1
ON	0	1	0	1

The DT531 decodes the TS16 CAS code such that if A bit is zero, 'T' lead output is set ON; and if A bit is one, 'T' lead output is set OFF.

Two debouncing options are provided at the CAS input. Option one: no debouncing of the A bit of TS16. Option two: approximately 6ms of debouncing of the A bits received at the channel card.

2. Operation

Digital data is dropped from the selected timeslots into a buffer store. This data is then clocked out from the store to the RD output using the Nx64k clock derived from a Voltage Controlled Oscillator in a phase lock loop circuit. The frequency of the VCO is set up using Control port 1.

Data appearing on the SD input is clocked into the buffer store (providing the RS and TR inputs are in the 'ON' condition) by the derived Nx64k clock. Data is then clocked out at the optimum time using the normal multiplexer PCM system timing. The timeslots to be used can either be consecutive or random in ascending order, i.e. a selection of timeslots could be:

TS1, TS5, TS14, TS27 for a 256kit/s circuit.

The card may be operated in a data link only mode where the state of the control signal inputs are ignored.

3. Specifications

Data Rate: Selectable in 64kbit/s steps 128kbit/s to 1984kbit/s.

Performance: Meets EIA Recommendation RS449 for data and timing signals.

Interface Levels: Selectable to CCITT Recommendations V.11 or V.35 (Red book).

Delay: The delay contributed by the card is 250 μ s for send data and 125 μ s for receive data.

Power Requirement: 4 Watts per card.

4. Loopback

When the Nx64k card is operated in a loop, data appearing on the SD input is looped back via the interface circuits to the RD output, and data dropped from the PCM towards RD is looped back and re-inserted into the PCM stream. Data dropped from the PCM will be inserted back into the same timeslots, however the data will be subject to a bit shift i.e. byte alignment in the timeslots will not be maintained.

5. Switch and Link Settings

	SW to the front of card	SW to the rear of card
SW12	8k1 Off	8k1 selected
SW13	8k2 Off	8k2 selected
SW1	Normal send data clock	Inverted send data clock
SW2	DCE	DTE
SW3	RS449	Data link only*

S4 to S11 and S14, S15 selects V.35 or V.11 Interface levels as follows:

S4 to S15 to the rear = V.35

S4 to S15 to the front = V.11

*SW3 - DT530 mode only

JP1 Position

1-2 PLB 3b (referenced to multiplexer backplane) connected to GND
2-3

JP 2 and 3 Position Data invert to and from the backplane.

1-2* Invert

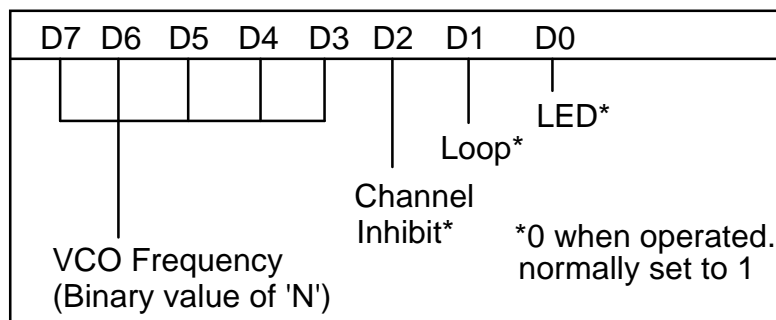
2-3 No invert

* Position 1-2 should be used for point-to-point operation with Issue 2 DT530 PCBs, or later.

6. Control Ports

6.1.1 Control Port 1

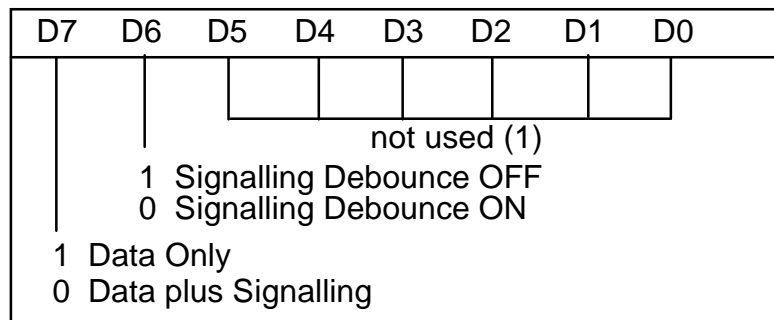
Control port 1 provides the following functions:



The VCO frequency is set up using Bits D3 to D7 of Control Port 1. This is the 'N' value, i.e. the number of timeslots.

RATE kbit/s	TIMESLOTS	D7	D6	D5	D4	D3
128	2	0	0	0	1	0
192	3	0	0	0	1	1
256	4	0	0	1	0	0
320	5	0	0	1	0	1
384	6	0	0	1	1	0
448	7	0	0	1	1	1
512	8	0	1	0	0	0
576	9	0	1	0	0	1
640	10	0	1	0	1	0
704	11	0	1	0	1	1
768	12	0	1	1	0	0
832	13	0	1	1	0	1
896	14	0	1	1	1	0
960	15	0	1	1	1	1
1024	16	1	0	0	0	0
1088	17	1	0	0	0	1
1152	18	1	0	0	1	0
1216	19	1	0	0	1	1
1280	20	1	0	1	0	0
1344	21	1	0	1	0	1
1408	22	1	0	1	1	0
1472	23	1	0	1	1	1
1536	24	1	1	0	0	0
1600	25	1	1	0	0	1
1664	26	1	1	0	1	0
1728	27	1	1	0	1	1
1792	28	1	1	1	0	0
1856	29	1	1	1	0	1
1920	30	1	1	1	1	0
1984	31	1	1	1	1	1

6.1.2 Control Port 2

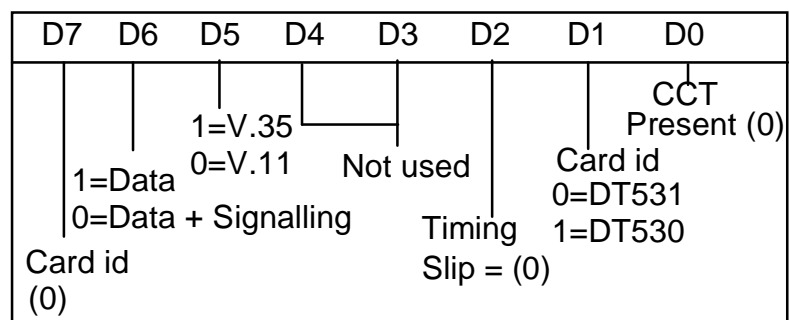


TS16 can be allocated as a data channel when in 'Common Channel Signalling' mode. TS16 must not be allocated to the card when the multiplexer is in 'Channel Associated Signalling' mode as data will be lost.

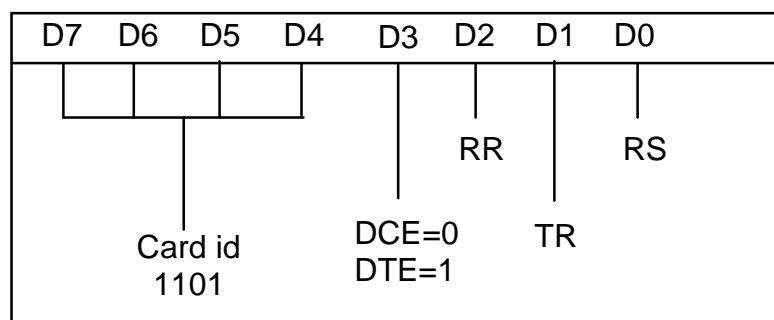
7. Status Ports

The status ports are used to show the current running condition of the circuit and to display the card identity. These are displayed as shown below:

Status Port 1



Status Port 2



8. Connections

Connection to the Nx64k card is via the 96-way DIN plug on the multiplexer. There are two different cabling requirements, one for V.11 levels and one for V.35 levels depending upon the requirement.

The connections for the RS449 V.11 levels are as follows:

TITLE	PIN NO	TITLE	PIN NO	CIRCUIT
RT(B) o/p	32b (50)	RT(A)	32c (25)	115
ST(B) o/p	30b (48)	ST(A)	30c (23)	114
TT(B) i/p	28b (46)	TT(A)	28c (21)	113
ETH	26b -	SG	26c -	102
RR(B) o/p ²	24b (44)	RR(A)	24c (19)	109
CS(B) o/p	22b (42)	CS(A)	22c (17)	106
SD(B) i/p	20b (40)	SD(A)	20c (15)	103
ETH	18b -	SG	18c -	102
DM(B)	16b (38)	DM(A)	16c (13)	107
TR(B) i/p ¹	12b (34)	TR(A)	12c (9)	108
ETH	10b -	SG	10c -	102
RD(B) o/p	8b (32)	RD(A)	8c (7)	104
RS(B) i/p	4b (28)	RS(A)	4c (3)	105
ETH	2b (26)	SG	2c (1)	102
SIGNAL GND	3b (27) ³			

The connections when using the V.35 levels are as follows:

TITLE	PIN NO.	TITLE	PIN NO.	CIRCUIT
RT(B) o/p	31b (49)	RT(A)	31c (24)	115
ST(B) o/p	29b (47)	ST(A)	29c (22)	114
TT(B) i/p	27b (45)	TT(A)	27c (20)	113
ETH	26b -	SG	26c -	102
SD(B) i/p	19b (39)	RR(V28) o/p ²	23c (18)	109
ETH	18b -	CS(V28) o/p	21c (16)	106
ETH	10b -	SD(A)	19c (14)	103
RD(B) o/p	7b (31)	SG	18c -	102
ETH	2b (26)	DM(V28) i/p	15c (12)	107
SIGNAL GND	3b (27) ³	TR(V28) ¹	11c (8)	108
		SG	10c (9)	102
		RD(A)	7c (6)	104
		RS(V28) i/p	3c (2)	105
		SG	2c (1)	102

Numbers shown above in brackets are those on the 50 way Amphenol female connector fitted to the universal I/O adapter DT280, or on the 2100 multiplexer.

Pin 1c is the bottom right-hand pin when viewed from the rear of the DIN connector.

Notes:

1. 'TR' = 'C'
2. 'RR' = 'I'
3. Signal Ground is selectable via JP1 pins 1 and 2

