

# **Quad 64k V.35 Data Card Reference Manual**

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## STATUTORY NOTICES

### APPROVALS

The Quad V.35 Data Card DT561 is approved for indirect connection to Telecommunications Systems under the General Approval Number NS/G/1234/J/100003. This card does not contain any isolation barriers, and any apparatus connected to it must conform to the requirements of the General Approval.

The safety status of the interface is SELV.



Case Technology Ltd declare that this product conforms with the protection requirements of Council Directive 89/336/EEC on the approximation of the laws of the member states relating to electromagnetic protection.

This equipment has been tested using shielded cables supplied by Case Technology Ltd. These cables, or equivalents, must be used to ensure compliance with this declaration.

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All PCB assemblies contain Electrostatic Sensitive Devices (ESDs) which may be permanently damaged if incorrectly handled. This equipment must be handled in accordance with BS5783 code of practice for the handling of electrostatic sensitive devices.

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# Quad 64k V.35 Data Card

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## 1. Description

The Quad 64k V.35 data card, DT561, operates as a Data Circuit-Terminating Equipment (DCE) to interface between four 64kbit/s Data Terminating Equipments (DTE) and channel timeslots in a 30/31 channel 2048kbit/s PCM stream.

Each interface provides the following V.28 input and output control lines:-

102		Signal Ground
105	RTS	Ready to Send (input)
106	RFS	Ready for Sending (output)
107	DSR	Data Set Ready (output)
109	DCRLSD	Data Circuit Receive Line Signal Detect (output)

The following V.35 data and clock lines are provided:-

103	TD	Transmit Data (input)
104	RD	Receive Data (output)
114	TCK	Transmit Timing (DCE) (output)
115	RCK	Receive Timing (DCE) (output)

## 2. Operation

The card drops digital data from the selected timeslot into a buffer store which is then clocked on to the RD output at 64kbit/s. Timing outputs are derived from the multiplexer 2048kbit/s clock. Signalling information is dropped from timeslot 16 for the associated timeslot, and the staticised data is decoded and presented at the output as DCRLSD.

Data appearing at the TD input may be sampled on either edge of the 64kbit/s clock by link selection before being fed into a buffer store ready for insertion into the PCM stream.

Signals appearing on the RTS input are encoded and inserted into the next associated timeslot 16.

**NOTE:** Because of the 500Hz TS16 signalling rate in the PCM stream and buffer stores on the data card, a change at the RTS input occurring in time with a particular data bit at the TD input on a local data card, may not appear until 136 clocks or 2.2ms later than the data bit when the two signals appear at the RD and DCRLSD outputs on a remote data card.

### **3. Specifications**

Data Rate:	64kbit/s
Number of Circuits:	4
Interface:	DCE
Electrical Levels:	Data and timing V.35 Control lines V.28
Delay:	The delay contributed by this card is 130 $\mu$ s for Transmit data and 4 $\mu$ s for Receive data.
Power Requirements:	4 Watts per card

### **4. Loop back**

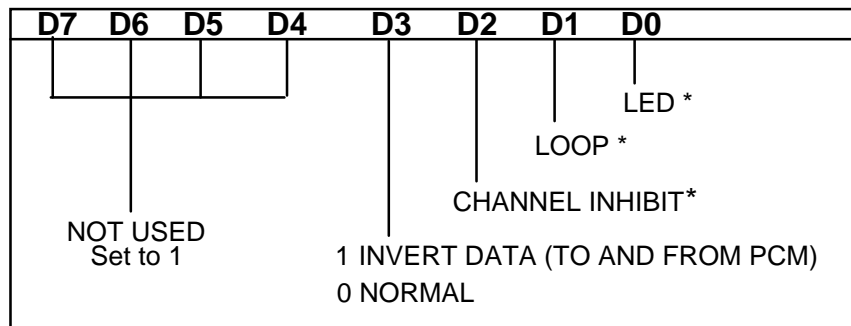
Test loops to CCITT recommendation X150 type 3c and 2b can be selected by the multiplexer control software. Loop back is enabled in both directions, i.e. signals appearing on the TD and RTS inputs are returned via the interface circuits on the RD and DCRLSD outputs respectively. Similarly, incoming signals from the PCM stream towards circuits RD and DCRLSD are looped back to the PCM stream.

**Note:** Whilst in loop, only recognised TS16 codes will be looped back into the PCM.

## 5. Control Port Functions

Only control port 1 is used by this card.

The functions are:-



\* D2, D1 and D0 are active when low (0).

The normal operating condition is:- 11110111B

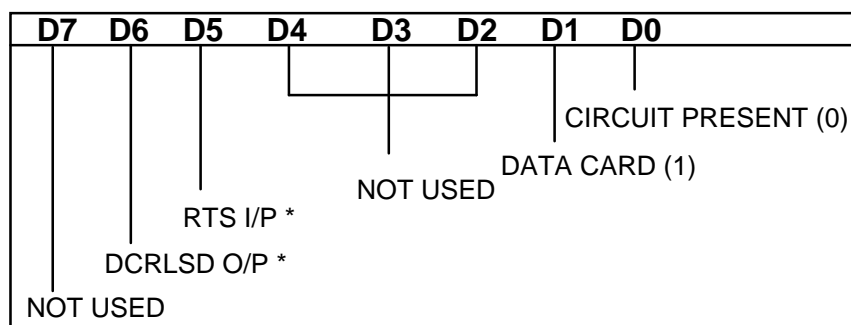
In this mode, a 1 at the V.35 input is transmitted as a 1 in the PCM, hence an open circuit will cause FFH to be transmitted in the PCM and presented at the V.35 output.

## 6. Status Port Facilities

The status bytes are monitored from within the multiplexer maintenance software.

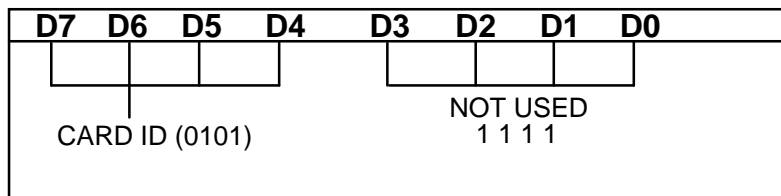
The facilities are as follows:-

### Status Port 1



\* '0' = ON, '1' = OFF.

## Status Port 2



## 7. Link Options

The links on the card are set for clocking the V.35 Transmit Data onto the card. The normal position is towards the top of the board. Changing the link inverts the clock edge, this facility may be used to compensate for delays in cables and DTEs.

LK1=CCT1

LK2=CCT2

LK3=CCT3

LK4=CCT4

## 8. Switch Operation

A switch provided at the front of the board that allows each circuit to be selected for either data link only, switch 'open' or data and control, switch 'closed'. When data and control is selected, RTS is used to control the RFS output and provide the RTS signal transmitted to the remote equipment via the PCM. The RTS signal received from the remote equipment is used to clamp the received data to all 1s (when off) and to drive the DCRLSD output. DSR is controlled by channel inhibit. In data link only mode, both the RTS input and the remote RTS signal received from the PCM are assumed to be 'ON'. This facility may be used to enable inter networking with other interfaces and for non CAS systems.

## **9. Inter networking**

This card is capable of inter networking with all universal data card modules at 64k only, no byte timing, data link only. In addition the card will also inter network with the DT520 (Quad 64k X.21) for data and control. When inter networking with the DT520 or the DTE50 (Dual V.11 Universal Data), it is necessary to ensure that data is inverted to and from the PCM, hence Control port 1 should be set to FFH. For all other universal data modules DTE51, DTE53 and DTE54, no inversion is required and hence the control port should be set to F7H.

## 10. Connections

Interface connections to the card are via the back plane 96 way DIN I/O connector as shown below. Numbers in brackets are those on the Amphenol female connector fitted to the universal I/O adapter DT280.

Circuit	TITLE	Pin No.	TITLE	Pin No.
Cct 4	RD(B)	32b (50)	RD(A)	32c (25)
	RxCK(B)	31b (49)	RxCK(A)	31c (24)
	TxCK(B)	30b (48)	TxCK(A)	30c (23)
	RFS	29b (47)	DCRLSD	29c (22)
	TD(B)	28b (46)	TD(A)	28c (21)
	DSR	27b (45)	RTS	27c (20)
	* ETH	26b	SIG GND	26c
Cct 3	RD(B)	24b (44)	RD(A)	24c (19)
	RxCK(B)	23b (43)	RxCK(A)	23c (18)
	TxCK(B)	22b (42)	TxCK(A)	22c (17)
	RFS	21b (41)	DCRLSD	21c (16)
	TD(B)	20b (40)	TD(A)	20c (15)
	DSR	19b (39)	RTS	19c (14)
	* ETH	18b	SIG GND	18c
Cct 2	RD(B)	16b (38)	RD(A)	16c (13)
	RxCK(B)	15b (37)	RxCK(A)	15c (12)
	TxCK(B)	14b (36)	TxCK(A)	14c (11)
	RFS	13b (35)	DCRLSD	13c (10)
	TD(B)	12b (34)	TD(A)	12c (9)
	DSR	11b (33)	RTS	11c (8)
	* ETH	10b	SIG GND	10c
Cct 1	RD(B)	8b (32)	RD(A)	8c (7)
	RxCK(B)	7b (31)	RxCK(A)	7c (6)
	TxCK(B)	6b (30)	TxCK(A)	6c (5)
	RFS	5b (29)	DCRLSD	5c (4)
	TD(B)	4b (28)	TD(A)	4c (3)
	DSR	3b (27)	RFS	3c (2)
	* ETH	2b (26)	SIG GND	2c (1)

\* The earth is taken from the backplane to the chassis earth.

When viewed from the rear of the chassis, Pin 1a is the bottom left hand pin of the connector.

V.35 interface connections using cable assembly CNE220.

<b>Signal</b>		<b>34 Way MRAC Female</b>
EARTH		A
SIG. GND		B
RTS	<-	C
RFS	->	D
DSR	->	E
DCRLSD	->	F
TxD(A)	<-	P
TxD(B)	<-	S
RxD(A)	->	R
RxD(B)	->	T
RxCK(A)	->	V
RxCK(B)	->	X
TxCK(A)	->	Y
TxCK(B)	->	AA

> = OUTPUT FROM multiplexer  
< = INPUT TO multiplexer

