

ARQ5 Module Reference Manual

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WARNING

The DCX 860 and 870 incorporate a panel in front of the plug-in modules. This panel may only be removed by suitably qualified personnel for installation or maintenance purposes, and must be replaced afterwards. Removal under any other circumstance would invalidate any RFI (Radio Frequency Interference) and Safety Type Approvals.

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Published by Case Technology Technical Publications Department

Preface

This manual provides information for DCX network supervisors to operate, configure and test the ARQ5 module. It forms part of the DCX Systems Documentation, and refers to other manuals in the series. It assumes that you will already have some knowledge of the DCX system, obtained either from the System Documentation or from a Cray training course.

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1.1 The ARQ5 Module

The ARQ5 module may be used in some members of the DCX family including the 850, 860* and 870*, to provide the interface to the high speed composite link.

The module provides the assembly and disassembly of frames, with error control as the frames are transmitted across the link, and DCX mapping functions (850, 860 and 870 only) under control of a System Module or an NCAM device.

- * The DCX 860 and 870 are designed to be soft-configurable, and physical access to the plug-in cards is unnecessary. Full details are given in the DCX 860, 870, System Module and NCAM manuals. Physical access is prevented by a panel, which may only be removed by suitably qualified personnel for installation and maintenance purposes.

1.2 Specification Summary

Interface	CCITT V.24/V.28, EIA RS-232-C CCITT V.35 CCITT X.21/V.11, EIA RS-422 CCITT V.36/V.11	
Transmission	Based on HDLC protocol as defined in CCITT X.25 Level 2 Optional Extended Window operating mode	
Data rates		
Internal clock	1200, 1800, 2400, 3600, 4800, 7200, 9600, 14400, 19200, 57600, 76800 or 79200 bps	
External clock	Any rate up to 79200 bps	
Error protection	Automatic repeat on request using cyclic redundancy check to CCITT V.41	
Satellite working	Single hop satellite link at 79200 bps, double hop satellite link at 19200 bps or less. See Appendix B.	
Link Protocol compatibility		
Standard operating mode	ARQ1	Issue 7 onwards
	ARQ2	Issue 1 onwards
	ARQ4	Issue 1 onwards
	812	Issue 1 onwards
	815	Issue 5 onwards
	815SE	Issue 1 onwards
	817	Issue 1 onwards
	825 CLP	Issue 1 onwards
	825 OLP	Issue 2 onwards
	842	Issue 1 onwards
	844	Issue 1 onwards
Extended Window operating mode	ARQ2	Issue 1 onwards
	ARQ4	Issue 1 onwards
	842	Issue 2 onwards
	844	Issue 1 onwards

2.1 Functional Description

The ARQ5 module operates in full-duplex mode and performs a number of functions. The first is the assembly of low speed channel data into frames for transmission over the high speed link. This is done by a microprocessor, which also controls the overall operation of the module. The frame is constructed to a format similar to the High-level Data Link Control (HDLC) format of CCITT Recommendation X.25 Level 2, in which each frame includes a frame check sequence (FCS) of 16 bits.

The second function is error control of frames being transmitted over the high speed link, using Automatic Repeat on Request (ARQ) 'go back to N' error control procedures, following CCITT recommendation V.41.

The third function is STC map control (this is not provided on ARQ1, ARQ2, or ARQ3). The ARQ5 will perform STC mapping functions according to command packets received on channel 1 of the composite link, from a System Module, NCAM or some other suitable device. Such mapping can be done even if the ARQ5 has no defined device base and size in the current STC map, allowing access to the node from a remote device, to configure the node even from a cold start.

Figure 2-1 shows the functional sub-units of the ARQ5 module.

The ARQ5 module contains a 32K byte memory of which 1K byte stores the last eight frames transmitted (or optionally 8K stores the last sixty-four frames) for retransmission in case of error.

During normal operation each ARQ is sending frames to the other. Each transmitted frame includes its frame number, the data, the FCS and an acknowledgement of the last received frame.

The receiving end recomputes the FCS and, if correct, sends positive acknowledgement back to the transmitting end. However, if it detects an error (for example in Frame N), it sends a negative acknowledgement. This causes the transmitting end to retransmit frame N and all subsequent frames.

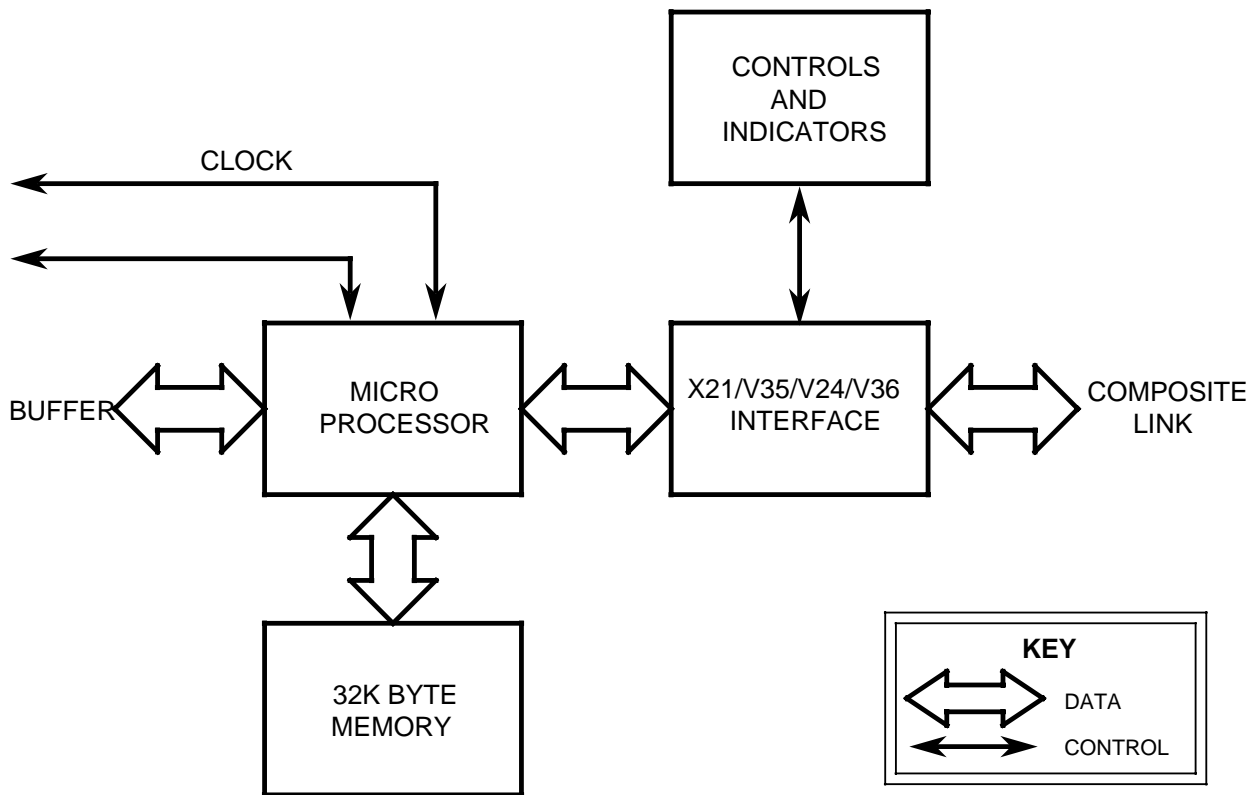


Figure 2-1 ARQ5 Module Simplified Block Diagram

The ARQ5 may take any ARQ position in the DCX frame, including the bus master slot (position 16 in 850, position 19 in 860). When in the bus master slot, ARQ5 provides the bus timing and control signals, unless a BAT card is installed in slot 1.

2.2 The Front Panel

The front panel of the ARQ5 card is illustrated in Figure 2-2. It has three pushbutton controls, ten general indicators and four interface indicators. The ON state of a red indicator is a warning sign and may indicate an error.

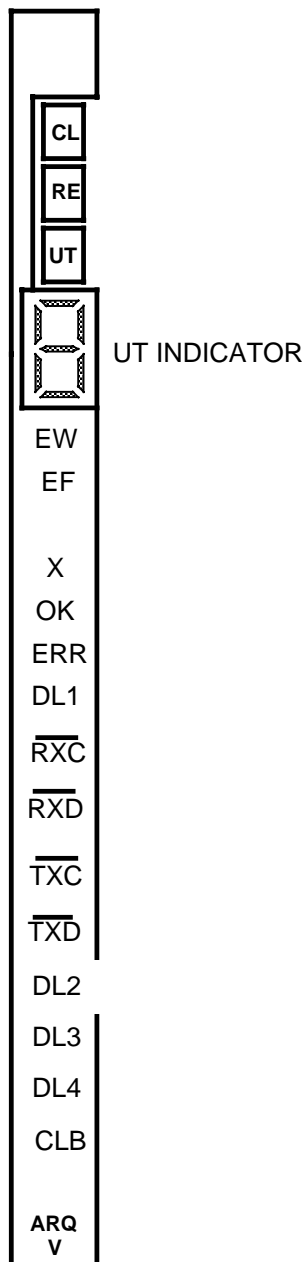


Figure 2-2 ARQ5 Module Front Panel

2.2.1 Controls

- CL** Composite loopback pushbutton (latching). When OUT, circuit is in normal mode. When IN, circuit is in loopback mode.
- RE** Reset pushbutton (momentary). When pressed, resets **ERR** indicator.
- UT** Utilisation pushbutton (latching). When OUT, utilisation indicator shows peak composite link utilisation. When IN, utilisation indicator shows current composite link utilisation.

2.2.2 Indicators

- UT** Alphanumeric display showing peak utilisation (maximum utilisation since **UT** pushbutton was last out) or current utilisation (average over last 20 frames) in tenths of the maximum frame length. Both transmitted and received data streams are checked, and the highest is displayed. During power-up, the letters 't' and 'u' are shown. It is also used for error indications; see Section 4.2.
- EW** Extended Window mode indicator. Lit when 64-frame window size is selected.
- EF** Only used for diagnostics.
- X** Error condition indicator. Lit when the software detects erroneous operating conditions.
- OK** Lit under normal operating conditions. Extinguished when the software detects erroneous operating conditions (i.e. when **X** is illuminated).
- ERR** Composite link error rate monitor. Illuminated when the error rate exceeds approximately 1 in 10^5 . Reset by RE button.
- DL1** Only used for diagnostics.
- DL2** Only used for diagnostics.
- DL3** Only used for diagnostics.
- DL4** Only used for diagnostics.
- CLB** Composite loopback indicator. Lit while composite loopback pushbutton is in the IN position (i.e. loopback enabled).

- $\overline{\text{RXC}}$** Receive Clock absent. When lit indicates loss of receive clock from modem.
- $\overline{\text{RXD}}$** Receive Data absent. When lit indicates loss of receive data from modem.
- $\overline{\text{TXC}}$** Transmit Clock absent. When lit indicates loss of transmit clock from modem or ARQ5 internal clock generator.
- $\overline{\text{TXD}}$** Transmit Data absent. When lit indicates loss of transmit data from DCX.

2.3 The Composite Link Port

The connector on the rear of the module is connected by cable to a 25-way D-type plug at the back of the parent DCX. Full details of this port and the cables required to connect the link are given in Appendix A.

3 Configuration and Installation

3.1 Configuration

The ARQ5 card has option straps and switches that must first be configured, before installing it into the parent DCX. The location of the straps and switches is given in Figure 3-1.

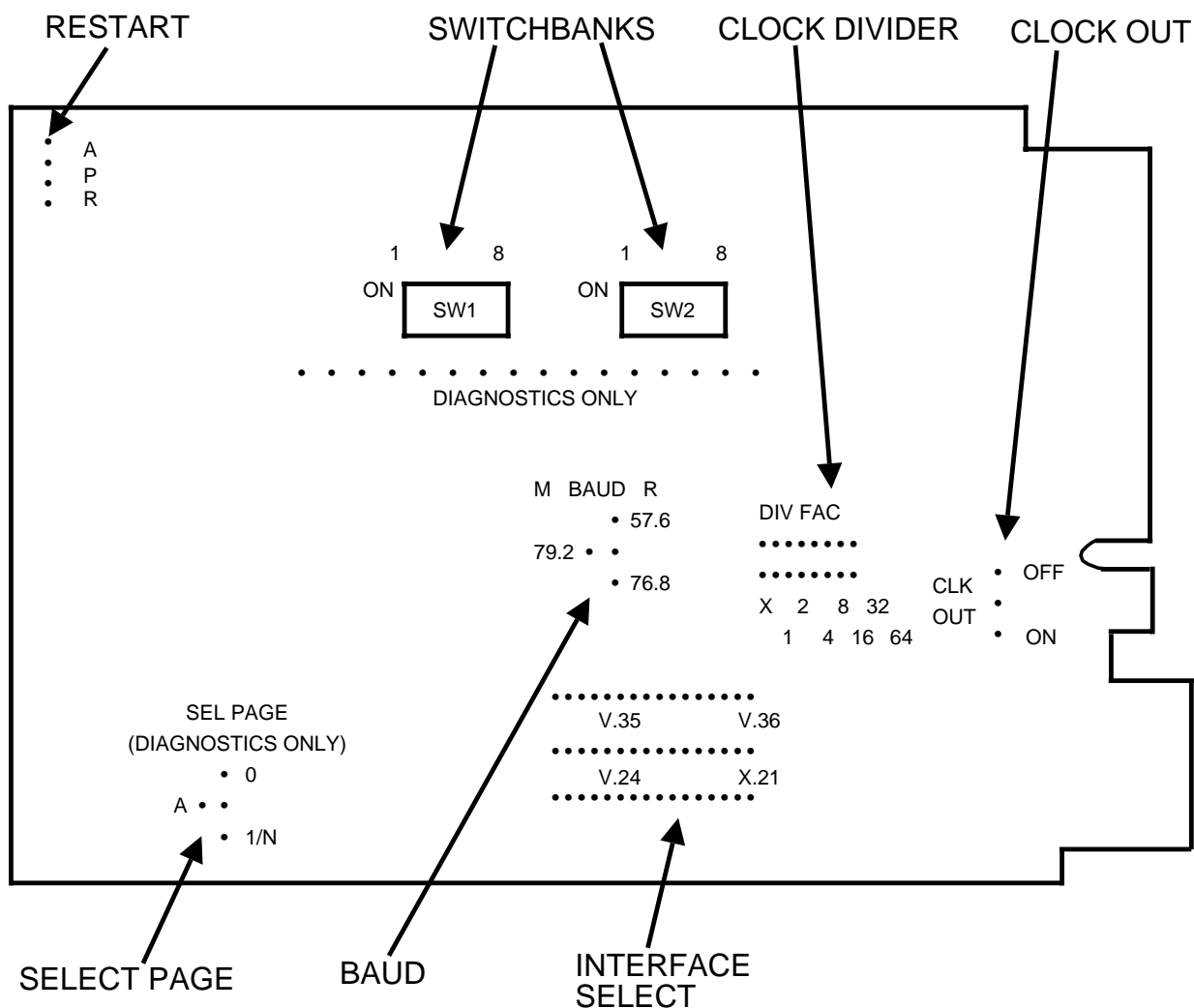


Figure 3-1 ARQ5 Option Strap and Switch Locations

3.1.1 Option Straps

The ARQ has six option straps, listed in Table 3-1 and explained below.

NAME	OPTION	POSITION
RESTART	Automatic restart	A
	Park - no action	P
	Reset	R
CLOCK DIVIDER	External clock	X
	79200 / 76800 / 57600	1
	39600 / 38400 / 28800	2
	19800 / 19200 / 14400	4
	9900 / 9600 / 7200	8
	4950 / 4800 / 3600	16
	2475 / 2400 / 1800	32
	1237 / 1200 / -----	64
BAUD	79200 master clock rate	79.2
	76800 master clock rate	76.8
	57600 master clock rate	57.6
CLOCK OUT	TX clock to modem	ON
	No TX clock to modem	OFF
SELECT PAGE	Factory test only	0
	Factory test only	A
	Normal operation	1/N
INTERFACE SELECT	V.35 interface selected	V.35
	V.36 interface selected	V.36
	V.24 interface selected	V.24
	X.21 interface selected	X.21

Table 3-1 Option Straps

RESTART

This strap should normally be set to automatic restart, position **A**, which will cause the module to reset itself automatically in the event of a software error. Position **P**, park, will cause the module to halt if a software error is detected. Position **R** will force a reset: the strap should not be left in this position.

Clock Source and Speed

ARQ5 timing can be derived either from the modem (external clock), or from an internal clock at a speed defined from a set of straps on the card. Two straps are used for these options:

CLOCK DIVIDER

This strap selects external clock or internal clock rate. The rate is obtained by dividing the master clock rate (set by the **BAUD** strap) by 1, 2, 4, 8, 16, 32 or 64. If the ARQ is configured for V.24 operation and internal clock is required, then the clock speed should not be set higher than 19800 bps. If the ARQ is configured for V.35 operation, the clock must be provided externally.

BAUD

This strap selects the internal master clock rate of 79200, 76800 or 57600 bps. It should be set in conjunction with the **CLOCK DIVIDER** strap to select the composite link speed when the internal clock is to be used.

For example to select an internal clock rate of 9600, set the **BAUD** strap to 76.8 and the **CLOCK DIVIDER** strap to 8.

CLOCK OUT

The TX clock may be fed to the modem by setting the strap to **ON**, or may be inhibited by setting it to **OFF**. Note that clocks are output on pins 4 and 17 whenever the **CL** pushbutton is IN, even if the **CLOCK OUT** strap is set to off.

SELECT PAGE

This strap should be in the 1/N position. Other positions are for factory test only.

INTERFACE SELECT

Four different standard interfaces are provided: V.36/V.11, V.35, X.21/V.11 (RS-422), and V.24/V.28 (RS-232-C).

Selection requires correct positioning of a header. The header goes in the 8 top left strap positions for V.35 composite link interface selection, the 8 top right strap positions for V.36, the 8 bottom left positions for V.24 or the 8 bottom right positions for X.21.

3.1.2 Option Switches

The ARQ5 has two switchbanks, SW1 and SW2, shown in Figure 2-1. The settings of these switchbanks are listed in Table 3-2 and explained below.

FEATURE	SETTING ON SW1							
	1	2	3	4	5	6	7	8
EXTENDED WINDOW MODE	D							
NORMAL WINDOW MODE	U							
LOW CHANNEL PRIORITY ENABLED	D							
LOW CHANNEL PRIORITY DISABLED	U							
LINK DOWN TIMEOUT: 40 (90) SECS							D	D
LINK DOWN TIMEOUT: 30 (80) SECS							D	U
LINK DOWN TIMEOUT: 20 (70) SECS							U	D
LINK DOWN TIMEOUT: 10 (60) SECS							U	U

FEATURE	SETTING ON SW2							
	1	2	3	4	5	6	7	8
DATA BYTE LIMIT PER CHANNEL:8	D	D						
DATA BYTE LIMIT PER CHANNEL:16	D	U						
DATA BYTE LIMIT PER CHANNEL:32	U	D						
DATA BYTE LIMIT PER CHANNEL:128	U	U						
NCAM MONITORING ENABLED			D					
NCAM MONITORING DISABLED			U					

U = UP D = DOWN

Table 3-2 Option Switches

NORMAL / EXTENDED WINDOW MODE

The normal mode is used for interworking with standard ARQ1, ARQ2, ARQ4 and ARQ5 modules over low delay circuits. The Extended Window mode is used with ARQ2/4 or ARQ5 modules for maintaining full performance over long delay (satellite) links.

The Extended Window option is enabled when this switch is DOWN. Normal operation takes place when the switch is UP.

PRIORITY

This option gives bandwidth priority to the low-ordered channel numbers. It is done by scanning for data, starting at channel 1, in two out of every three frames to be sent. On the third frame scanning for data starts at the next sequential channel each time, in a round-robin sequence. If there is no data to send on a channel, then the next sequential channel is scanned.

Priority is given to lower channel numbers when this switch is DOWN. Normal operation takes place when the switch is UP.

LINK DOWN TIMEOUT

The period that a link can be down before it is considered to be lost depends on the Normal/Extended Window mode strap. In Normal mode it allows for a period of 10, 20, 30 or 40 seconds. In Extended Window mode it allows for 60, 70, 80 or 90 seconds.

DATA LIMIT PER CHANNEL

The maximum number of data bytes assembled into a frame for each channel can be limited to 128 (i.e. full frame), 32, 16 or 8 bytes. Smaller frames give a steadier throughput to each channel. Limiting the data in this way will ensure that the data from a low volume device (e.g. a terminal) will not be held back by high volume devices (e.g. printers) filling every frame with their data.

SYSTEM MODULE/NCAM MONITORING

If this switch is DOWN, monitoring and execution of mapping control information from a System Module or NCAM card is enabled. This is fully explained in the System Module and NCAM manuals.

3.2 Installation

When the ARQ5 has been configured, it is ready to be installed in the parent unit (for appropriate slots, see the parent unit manual). However if it is not a known working module, it should first be tested by the procedure in Section 3.2.2. **WARNING:** for installation in DCX 860 or 870, see page 0-2.

3.2.1 Installation Procedure

1. Power down the parent DCX.
2. Insert the ARQ5 card in an ARQ slot.
3. Fit the appropriate cable from the card lower edge connector to the correct port connector aperture on the parent unit back panel.
 - In the DCX 836/850/860/870 use cable X840-400311. Unscrewing and swinging down the rear connector panel allows access to the card edge connector and frame.
4. Connect the composite link (see Appendix A).
5. Power up the parent DCX.

3.2.2 Checkout Procedure

1. If the Clock Divider strap (see Section 3.1.1) is set to External, move it to one of the Internal clock rate positions.
2. With power off, insert the card into any ARQ slot.
3. If a composite link cable is connected for this ARQ, disconnect it.
4. Power up the DCX and wait for the node to come up. When it is running, press the **CL** (composite loopback) pushbutton to latch it in. The **CLB** indicator and the **OK** indicator should both light.
5. Press the **CL** pushbutton again to release it. The **CLB** indicator should go out immediately, and the **OK** indicator should go out after the time set by the SW1 option switches 7 and 8.
6. If operations 4 and 5 were satisfactory, reinstate operations 1 and 3 if appropriate.

4 **Operation and Error Indications**

4.1 Normal Operation

No user action is required for the ARQ5 module to operate normally.

In normal operation the green **OK** indicator will be ON; the **X**, **ERR** and **CLB** indicators will be OFF; the composite link indicators will monitor the clock and data lines. The **UT** indicator will show composite link utilisation; it may be set to show either peak or current utilisation by means of the **UT** pushbutton.

4.2 Error Indications

UT indicator blank (other lights ON)	Suspect ARQ card.
UT indicator shows t or u except during power-up	Suspect ARQ card.
UT indicator shows E	Suspect ARQ card.
UT indicator shows □	Check composite link.
UT indicator shows ▣	Check Base and Size on 850/860/ 870 mapping.
ERR light on	Check composite link.
OK light off, X and one or more of RXC, TXC, RXD, TXD on	Attempt composite loopback test. If not accepted, or error persists in loopback mode, suspect ARQ card. If OK in loopback, check modems, cables etc.
UT indicator cycles through 0-t	Ensure that Select Page strap is in position 1/N; if it is, suspect ARQ card.

To clear the **ERR** indicator after the fault has been rectified press the **RE** button (except in DCX 860 or 870).

5.1 Composite Loopback Test

This test places the composite link in bidirectional loopback at the ARQ5 card. It assumes that the link is up and running and/or clocking arrangements are valid at both ends.

All channels on the link are looped back when the **CL** button is initially depressed. It is therefore wise to ensure that all users of the composite link are not actively working.

1. Turn DCX 850 Mode key to local.
2. Press **CL** pushbutton on ARQ5 card. The **CLB** indicator should light to show loopback operation.
3. Check data flow under loopback conditions. The **OK** indicator should come on if the ARQ5 is operating correctly.
4. If it is possible to check the remote ARQ **OK** indicator, it will be on only if both the remote ARQ and the composite link are operating correctly.
5. Press **CL** to terminate loopback (**CLB** goes out).
6. Turn Mode key counterclockwise.
7. If possible, do a similar loopback test at the remote ARQ.

Other methods of achieving composite loopback are described in the parent DCX, NCAM and System Module manuals.

A.1 Composite Link Interface

The ARQ5 composite link interface terminates in a 25-way D-type plug at the rear of the parent DCX. The interface signals conform to the interface selected by the 8-pin option plug on the ARQ5 card, and are listed in Table A-1.

PIN	SELECTED INTERFACE				SIGNAL DESCRIPTION
	V.24	V.35	V.36	X.21	
1		TXCA			Transmitter Clock
2		RXCA			Receiver Clock
3		RXDA			Received Data
4	CLKOUT			CLKA	Clock Out (A)
5				CA	Control (A)
6			TDA	TA	Transmit (A)
7	GND	GND	GND	GND	Signal Ground
8	TXD				Transmitted Data
9		TXDA			Transmitted Data (A)
10	RXC				Receiver Clock
11	TXC		TCA	SA	Transmitter Clock (A)/Signal Element Timing
12	RXD		RDA	RA	Received Data (A)
13			RCB	IA	Receiver Clock (B) /Indicator (A)
14		TXCB			Transmitter Clock (B)
15		RXCB			Receiver Clock (B)
16		RXDB			Received Data (B)
17				CLKB	Clock Out (B)
18				CB	Control (B)
19			TDB	TB	Transmitted Data (B)
20	RTS	RTS			Request To Send
21	DTR	DTR			Data Terminal Ready
22		TXDB			Transmitted Data (B)
23			RCA	IB	Receiver Clock (A)/Indicator (B)
24			TCB	SB	Transmitter Clock (B)
25			RDB	RB	Received Data (B)

Table A-1 ARQ5 Composite Link Interface

A.2 Cables

Connection from the parent unit to a modem is made using a cable appropriate to the interface type required, selected from those listed in Figures A-1 to A-4. Connection to another ARQ5, or an ARQ2/4, is made using the X.21 Crossover Cable (Figure A-5).

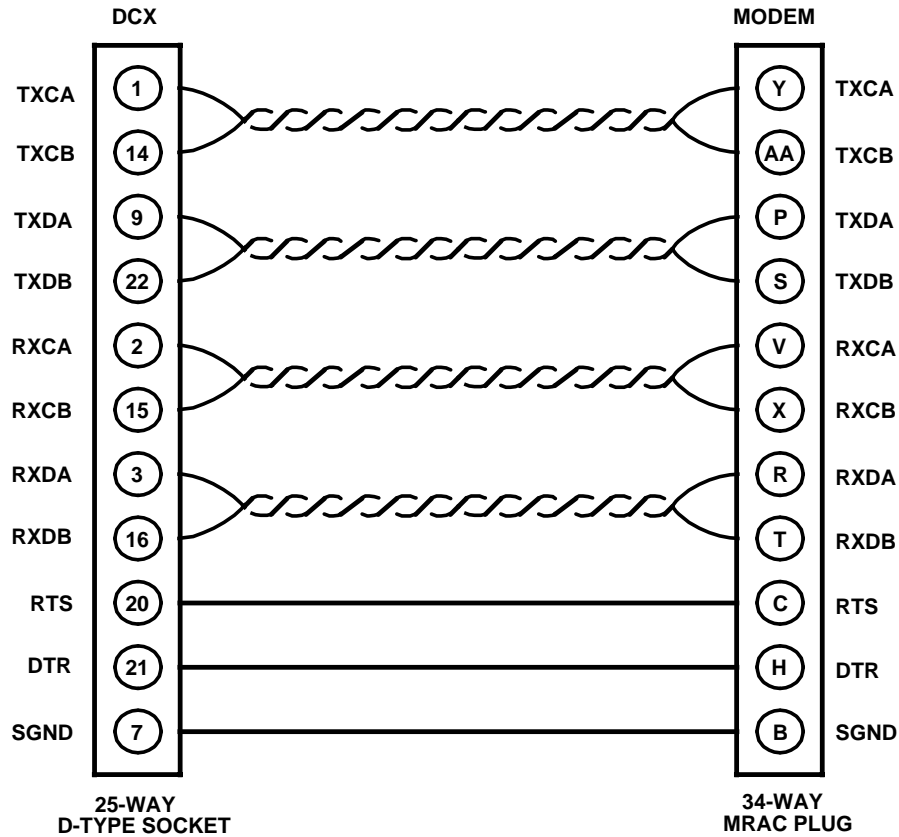


Figure A-1 V.35 Interface Cable X840-402611 (Datel Service) or X840-403011 (Kilostream Service)

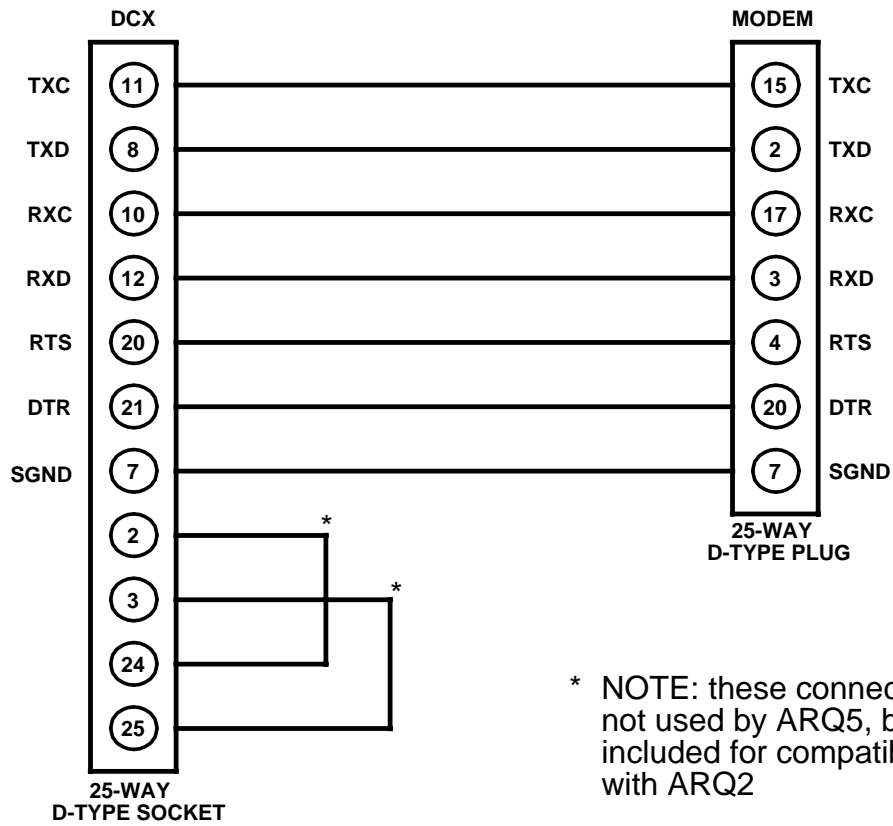


Figure A-2 V.24 Interface Cable X840-402811

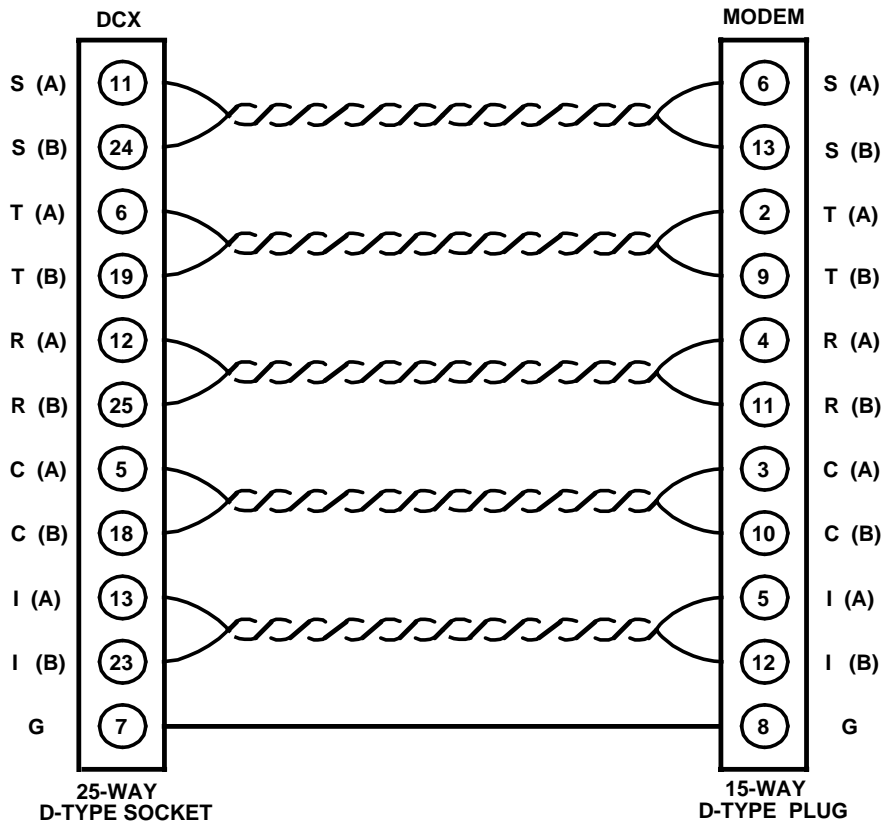


Figure A-3 X.21 Interface Cable X840-402711

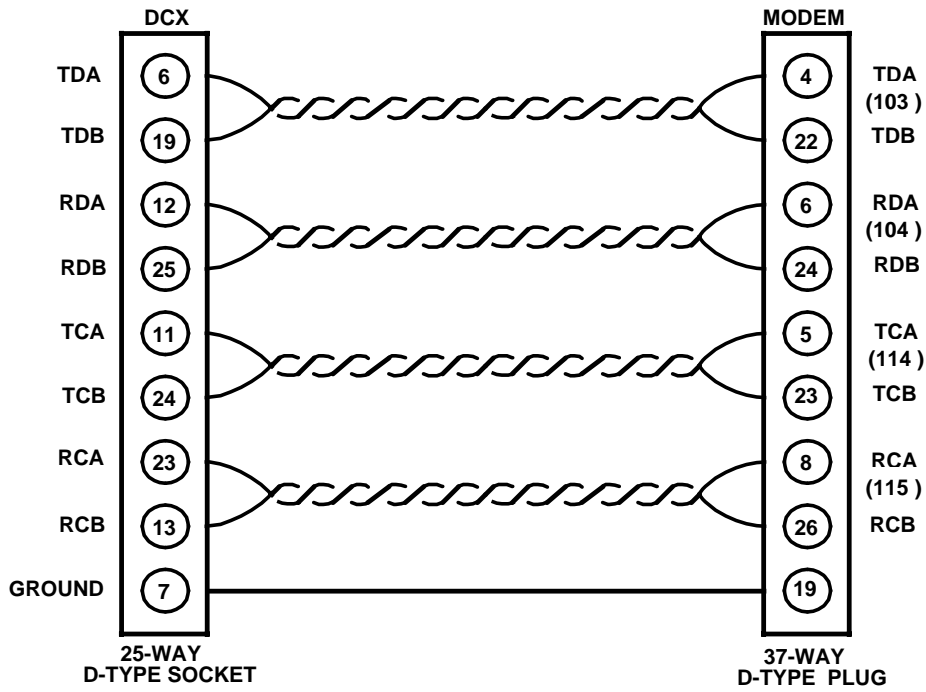


Figure A-4 V.36 Interface Cable X840-404911

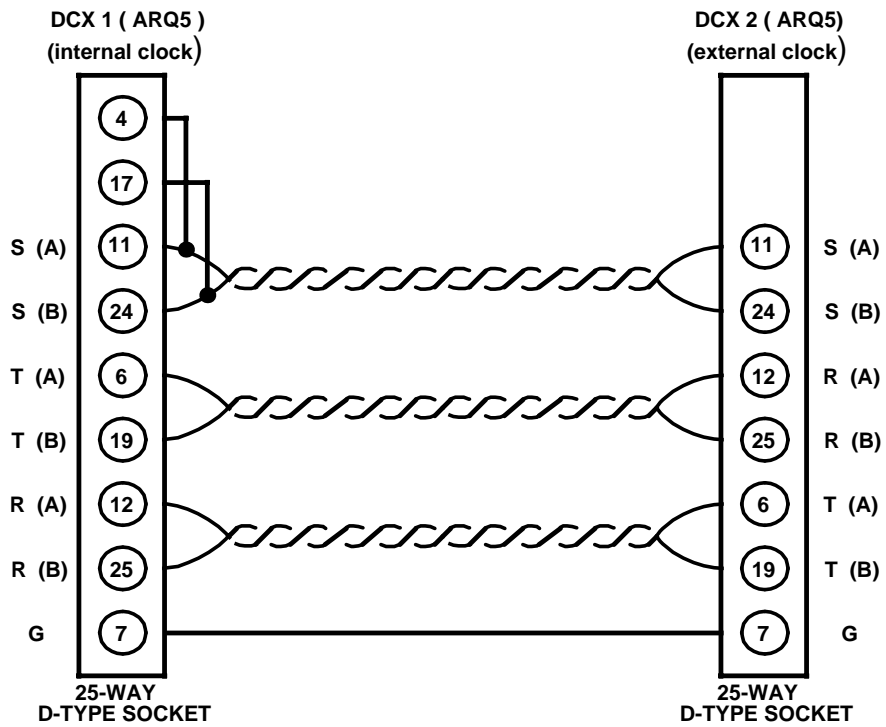


Figure A-5 X.21 Crossover Cable X840-404311

The information given in Section 1.2 concerning satellite working with extended windows is intended as a guide only. The table below shows the practical maximum propagation delay, from end to end, which the ARQ protocol can tolerate.

ARQ LINK SPEED	MAX. PROPAGATION DELAY
64 Kbps	750 MS
48 Kbps	760 MS
19200 bps	825 MS
9600 bps	925 MS

Table B-1 Maximum Propagation Delay

